IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent of:	Stasiak et al.
Patent No.:	7,034,332
Issued:	Apr. 25, 2006
Atty. Docket No.:	200206003-1
Title:	Nanometer-Scale Memory Device Utilizing Self-Aligned Rectifying Elements and Method of Making

OK to Enter
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SUBMISSION OF PRIOR ART UNDER 37 C.F.R. §1.501

Hon. Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir or Madam:

The undersigned herewith submits in the above-identified patent the following prior art (including copies thereof) which is pertinent and applicable to the patent and is believed to have a bearing on the patentability of at least claims 1, 2, 4, 7-9, 12, 18-20, and 22-27:

Lung, US 6,579,760, Jun. 17, 2003
Chou, US 5,772,905, Jun. 30, 1998

Lung in view of Chou renders obvious at least claims 1, 2, 4, 7-9, 12, 18-20, and 22-27 of US 7,034,332 B2 under 35 USC 103(a) as follows:

Regarding claim 1, Lung discloses a memory device, comprising: a substrate (100, Fig. 3); a plurality of self-aligned rectifying elements (selection diodes 28, Fig. 2, column 5, lines 1-19), having: a plurality of first electrode lines (135, 136, 137, Fig. 10) disposed over said substrate (100), a plurality of device structures (130) disposed on said plurality of first electrode lines forming said plurality of self-aligned rectifying elements (column 7, lines 18-20); a plurality of switching elements (phase change memory segments 30, Fig. 2), said switching elements disposed over and self-aligned in at least one direction with said device structures (column 5, lines 1-19); and a plurality of second electrode lines (138,

139) disposed over, electrically coupled to, and self-aligned to said switching elements, whereby a memory device is formed (Fig. 10).

Lung fails to disclose that the rectifying elements are nano-rectifying elements or that each device structure having at least one lateral dimension less than about 75 nanometers.

Chou is also related to electronic device manufacture (column 1, lines 28-31) and teaches a nanoimprint lithography system to pattern sub-25 nm features (column 2, lines 19-45).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to form the self-aligned rectifying elements of Lung of sub-75 nm dimensions using the nanoimprint lithography process of Chou.

The motivation for doing so would have been to produce a high device density at low manufacture cost as suggested by column 1, lines 32-40 of Chou.

Regarding claim 2, Lung discloses that said plurality of first electrode lines further comprises a plurality of first semiconductor lines including a dopant of a first polarity (column 2, lines 50-54).

Regarding claim 4, Lung discloses that said plurality of device structures further comprises a plurality of semiconductor device structures including a dopant of a second polarity, wherein each semiconductor device structure forms a semiconductor junction with one of said plurality of first semiconductor lines (column 2, lines 50-54). Lung does not disclose that said semiconductor junction having an area with at least one lateral dimension less than about 75 nanometers, however it would have been obvious to a person of ordinary skill in the art to form the semiconductor junction with an area having a lateral dimension less than 75 nanometers given the teachings of Chou to produce a high device density at low manufacture cost as suggested by column 1, lines 32-40 of Chou.

Regarding claim 7, Lung discloses said plurality of first semiconductor lines is formed on an insulating layer (101) formed on said substrate (100) (Fig. 3, column 5, lines 25-35).

Regarding claim 8, Lung discloses said insulating layer (101) is selected from the group consisting of SiOx, SixNy, SiOxNy, SixCy, and mixtures thereof (column 5, lines 27-28 teaches SiO2).

Regarding claim 9, Lung discloses said plurality of first electrode lines further comprises a plurality of metal electrode lines (column 5, lines 35-41), and wherein said plurality of device structures further comprises a plurality of semiconductor device structures including a dopant (column 2, lines 50-54), forming a plurality of Schottky barrier contacts between said plurality of metal electrode lines and

said plurality of semiconductor device structures (column 5, lines 54-57). Lung does not disclose that said Schottky barrier has an area with at least one lateral dimension less than about 75 nanometers, however it would have been obvious to a person of ordinary skill in the art to form the Schottky barrier with an area having a lateral dimension less than 75 nanometers given the teachings of Chou to produce a high device density at low manufacture cost as suggested by column 1, lines 32-40 of Chou.

Regarding claim 12, Lung discloses each switching element of said plurality of switching elements further comprises a phase change material (column 2, lines 55-57).

Regarding claim 18, Lung discloses each switching element of said plurality of switching elements further comprises a chalcogenide material (column 2, lines 55-57).

Regarding claim 19, Lung discloses said plurality of first electrode lines (135, 136, 137) are substantially parallel to each other (Fig. 10).

Regarding claim 20, Lung discloses said plurality of switching elements (130) further comprises a plurality of switching lines substantially parallel to each other (Fig. 10).

Regarding claim 22, Lung fails to disclose that each device structure has an area less than about 5,625 square nanometers. However, it would have been obvious to a person of ordinary skill in the art to form a device area less than 5,625 square nanometers given the teachings of Chou to produce a high device density at low manufacture cost as suggested by column 1, lines 32-40 of Chou.

Regarding claim 23, Lung discloses a memory device, comprising: a substrate (100); a first plurality of conductive lines (135, 136, 137) substantially parallel to each other disposed on said substrate; a plurality of semiconducting junctions (isolation diodes 26) formed on said first plurality of conductive lines; a second plurality of conductive lines (138, 139) substantially parallel to each other and substantially mutually orthogonal to said plurality of semiconducting lines; and a storage media (130) disposed between said first and said second conductive lines and electrically coupled to said junctions and said second plurality of conductive lines (Fig. 10).

Lung fails to disclose that the junctions have at least one lateral dimension less than about 75 nanometers.

Chou is also related to electronic device manufacture (column 1, lines 28-31) and teaches a nanoimprint lithography system to pattern sub-25 nm features (column 2, lines 19-45).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to form the junctions of Lung of sub-75 nm dimensions using the nanoimprint lithography process of Chou.

The motivation for doing so would have been to produce a high device density at low manufacture cost as suggested by column 1, lines 32-40 of Chou.

Regarding claim 24, Lung discloses a memory device comprising: a substrate (100); means for rectifying (isolation diode 26) including a first plurality of conductive lines (135, 136, 137) substantially parallel to each other disposed on said substrate, said means for rectifying self-aligned with said plurality of conductive lines (column 7, lines 18-20); means for storing a data bit in each of a plurality of storage elements (phase change cells, column 6, lines 20-31) disposed over said first plurality of conductive lines (135, 136, 137) and self-aligned to said means for rectifying (column 7, lines 18-23); and means for electrically addressing said plurality of storage elements (150-155), wherein each storage element self-aligned with said means for electrically addressing (Fig. 11), and wherein each intersection of said means for electrically addressing and said first plurality of conductive lines defines a logic cell, of a memory structure (column 3, lines 52-55).

Lung fails to disclose that the means for rectifying have at least one lateral dimension less than about 75 nanometers.

Chou is also related to electronic device manufacture (column 1, lines 28-31) and teaches a nanoimprint lithography system to pattern sub-25 nm features (column 2, lines 19-45).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to form the means for rectifying of Lung of sub-75 nm dimensions using the nanoimprint lithography process of Chou.

The motivation for doing so would have been to produce a high device density at low manufacture cost as suggested by column 1, lines 32-40 of Chou.

Regarding claim 25, Lung discloses a memory device, comprising: a substrate (100); a plurality of rectifying structures (isolation diodes 26), disposed on said substrate, said rectifying structures form an $i \times j$ array, wherein i and j are integer values (Fig. 2 illustrates a 2x2 array); a plurality of storage media elements (phase change memory segments), each storage media element disposed on and electrically coupled to one of said rectifying structures (Fig. 2); and a plurality of electrical conductor lines (135-139, Fig. 10) disposed on and electrically coupled to said plurality of storage media elements (130), wherein each storage media element is self-aligned to one of said rectifying structures and is self-aligned to one of said electrical conductor lines (column 3, lines 6-17).

Lung fails to disclose that each rectifying structure and storage media element has at least one lateral dimension less than about 75 nanometers

Chou is also related to electronic device manufacture (column 1, lines 28-31) and teaches a nanoimprint lithography system to pattern sub-25 nm features (column 2, lines 19-45).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to form the rectifying structure and storage media of Lung of sub-75 nm dimensions using the nanoimprint lithography process of Chou.

The motivation for doing so would have been to produce a high device density at low manufacture cost as suggested by column 1, lines 32-40 of Chou.

Regarding claim 26, Lung discloses a memory device, comprising: a substrate (100); a plurality of self-aligned rectifying elements (isolation diodes 26, Fig. 2), having: a plurality of first conductive lines (135, 136, 137) disposed over said substrate, a plurality of device structures (130) disposed on said plurality of first conductive lines, wherein the combination of said first conductive lines and said device structures forms said plurality of rectifying elements (column 7, lines 18-20, the isolation diodes are the selection devices); a plurality of switching elements (phase change segments, Fig. 2), each switching element disposed on and electrically coupled to one of said plurality of device structures (column 6, lines 19-31); and a plurality of second conductive lines (138, 139), said second conductive lines electrically coupled to said plurality of switching elements, each second conductive line intersects with at least one first conductive line (Fig. 10, column 7, lines 18-23), wherein each rectifying element is substantially facially coextensive, coincident, and coplanar with one of said plurality of first conductive lines and one of said plurality of switching elements (as illustrated in Fig. 10).

Lung fails to disclose that each first conductive line and device structure having at least one lateral dimension less than about 75 nanometers.

Chou is also related to electronic device manufacture (column 1, lines 28-31) and teaches a nanoimprint lithography system to pattern sub-25 nm features (column 2, lines 19-45).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to form the first conductive lines and device structures of Lung of sub-75 nm dimensions using the nanoimprint lithography process of Chou.

The motivation for doing so would have been to produce a high device density at low manufacture cost as suggested by column 1, lines 32-40 of Chou.

Regarding claim 27, Lung discloses a memory device, comprising: a substrate (100); a plurality of semiconducting lines (135, 136, 137) including a dopant of a first polarity (column 2, lines 50-54) said semiconducting lines substantially parallel to each other and disposed over said substrate (Fig. 10); a plurality of semiconducting structures including a dopant of a second polarity disposed on said plurality of semiconducting lines (column 2, lines 50-54); a plurality of junctions (130) formed between said lines and said semiconducting structures; a switching element (chalcogenide phase change material) disposed on and electrically coupled to said semiconducting structures (column 7, lines 18-23); and a plurality of electrical conductors (138, 139) substantially parallel to each other, coupled to said storage media and substantially mutually orthogonal to said plurality of semiconducting lines (Fig. 10).

Lung fails to disclose that said junctions have at least one lateral dimension less than about 75 nanometers.

Chou is also related to electronic device manufacture (column 1, lines 28-31) and teaches a nanoimprint lithography system to pattern sub-25 nm features (column 2, lines 19-45).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to form the junctions of Lung of sub-75 nm dimensions using the nanoimprint lithography process of Chou.

The motivation for doing so would have been to produce a high device density at low manufacture cost as suggested by column 1, lines 32-40 of Chou.

CERTIFICATE OF SERVICE

I hereby certify on Oct 1, 2010, that a true and correct copy of the foregoing "Submission of Prior Art" was mailed by first-class mail, postage paid, to:

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Intellectual Property Administration
3404 E. Harmony Road
Mail Stop 35
FORT COLLINS CO 80528

CONCLUSION

For the reasons presented above Lung, which was not cited during the patent examination of US 7,034,332, is seen to have bearing on the patentability of at least claims 1, 2, 4, 7-9, 12, 18-20, and 22-27 of US 7,034,332 as prior art.

All correspondence may be made to the following address:

Blaise Mouttet
4201 Wilson Blvd 110-364
Arlington, Va 22203

Respectfully Submitted,

Bl. Mou 9/30/2010

Blaise Mouttet

Doc Code: IDS

Document Description: Information Disclosure Statement filed

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37 CFR 1.501 INFORMATION DISCLOSURE CITATION IN A PATENT (Sheet 1 of 1)	Docket Number (Optional) 200206003-1	Patent Number 7034332
	Applicant Stasiak et al.	
	Issue Date Apr. 25, 2006	Art Unit 2891

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6579760	6/03	Lung			
	5772905	6/98	Chou			

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER	DATE CONSIDERED

This collection of information is required by 37 CFR 1.501. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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37 CFR 1.501
US 7,034,332

US006579760B1

(12) **United States Patent**
Lung

(10) **Patent No.: US 6,579,760 B1**
(45) **Date of Patent: Jun. 17, 2003**

(54) **SELF-ALIGNED, PROGRAMMABLE PHASE CHANGE MEMORY**

(75) Inventor: **Hsiang-Lan Lung**, Hsinchu (TW)

(73) Assignee: **Macronix International Co., Ltd.**, Hsinchu (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/108,658**

(22) Filed: **Mar. 28, 2002**

(51) **Int. Cl.**[7] **H01L 21/336**

(52) **U.S. Cl.** **438/257**; 438/308; 365/103; 365/63; 365/51

(58) **Field of Search** 438/257, 95, 128, 438/237, 238, 466, 597; 365/103–100, 113, 163

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Blake Thesis, "*Investigation of $Ge_2Te_2Sb_5$ Chalcogenide Films for Use as an Analog Memory*", AFIT/GE/ENG/00M–04,Mar. 2000, 121 pages.

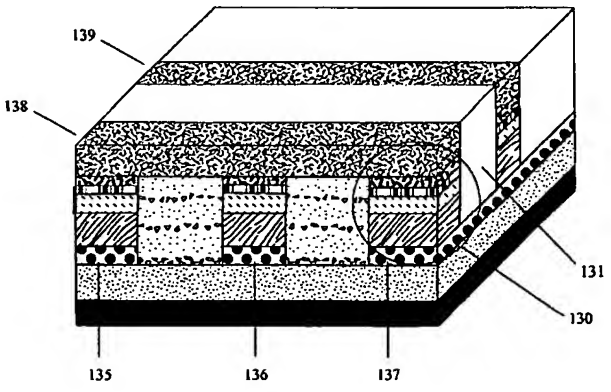
* cited by examiner

Primary Examiner—David Nelms
Assistant Examiner—D Le
(74) *Attorney, Agent, or Firm*—Mark A. Haynes; Haynes Beffel & Wolfeld LLP

(57) **ABSTRACT**

A self-aligned, nonvolatile memory structure based upon phase change materials, including chalcogenides, can be made with a very small area on an integrated circuit. The manufacturing process results in self-aligned memory cells requiring only two array-related masks defining the bit lines and word lines. Memory cells are defined at intersections of bit lines and word lines, and have dimensions that are defined by the widths of the bit lines and word lines in a self-aligned process. The memory cells comprise structures including a selection device, a heating/barrier plate layer and a phase change memory element, vertically arranged at the intersections of the bit lines and word lines.

20 Claims, 12 Drawing Sheets



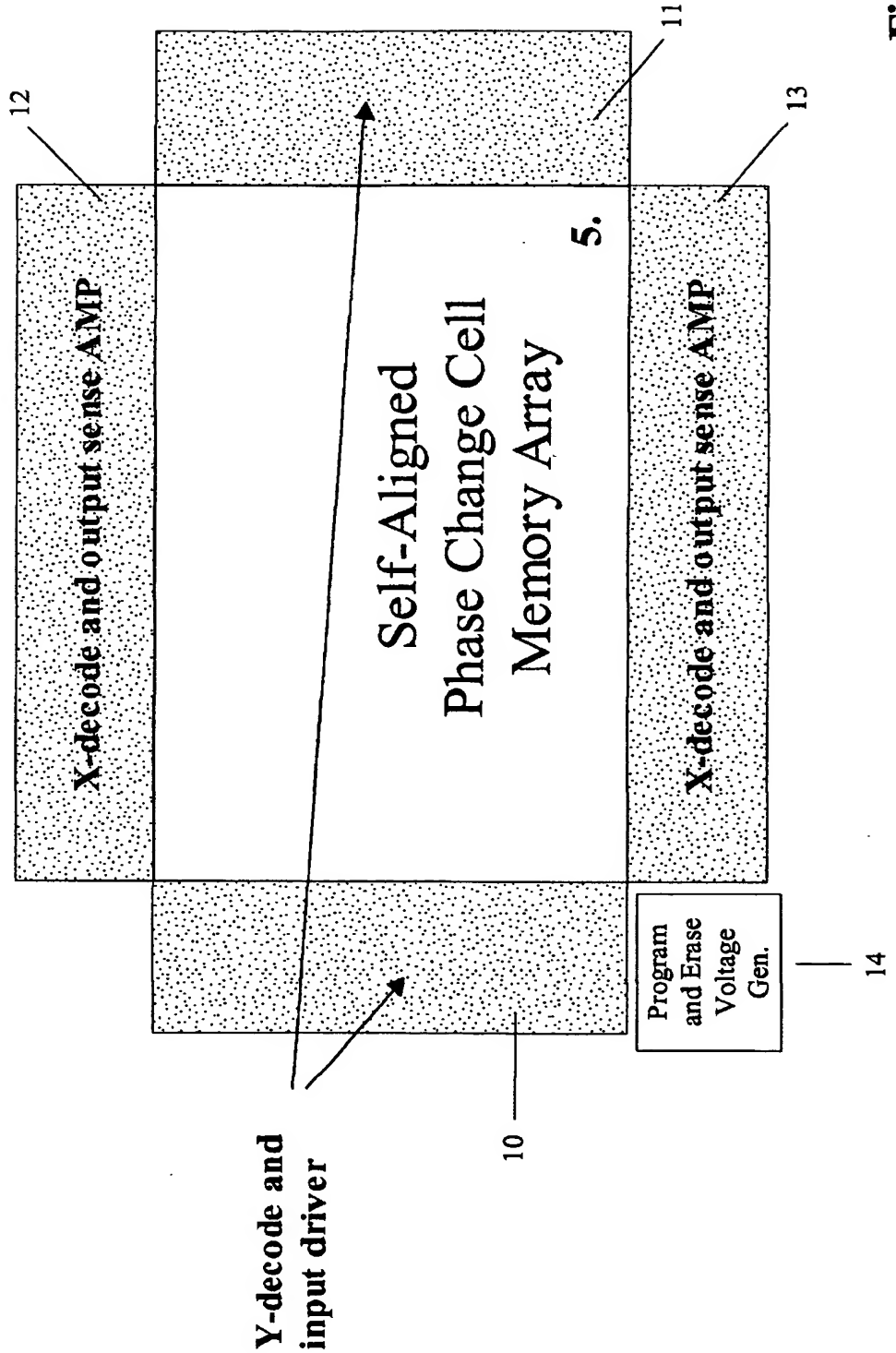

11
12
13
X-decode and output sense AMP
Self-Aligned
Phase Change Cell
Memory Array
5.
X-decode and output sense AMP
Program
and Erase
Voltage
Gen.
14
Y-decode and
input driver
10

Fig. 1

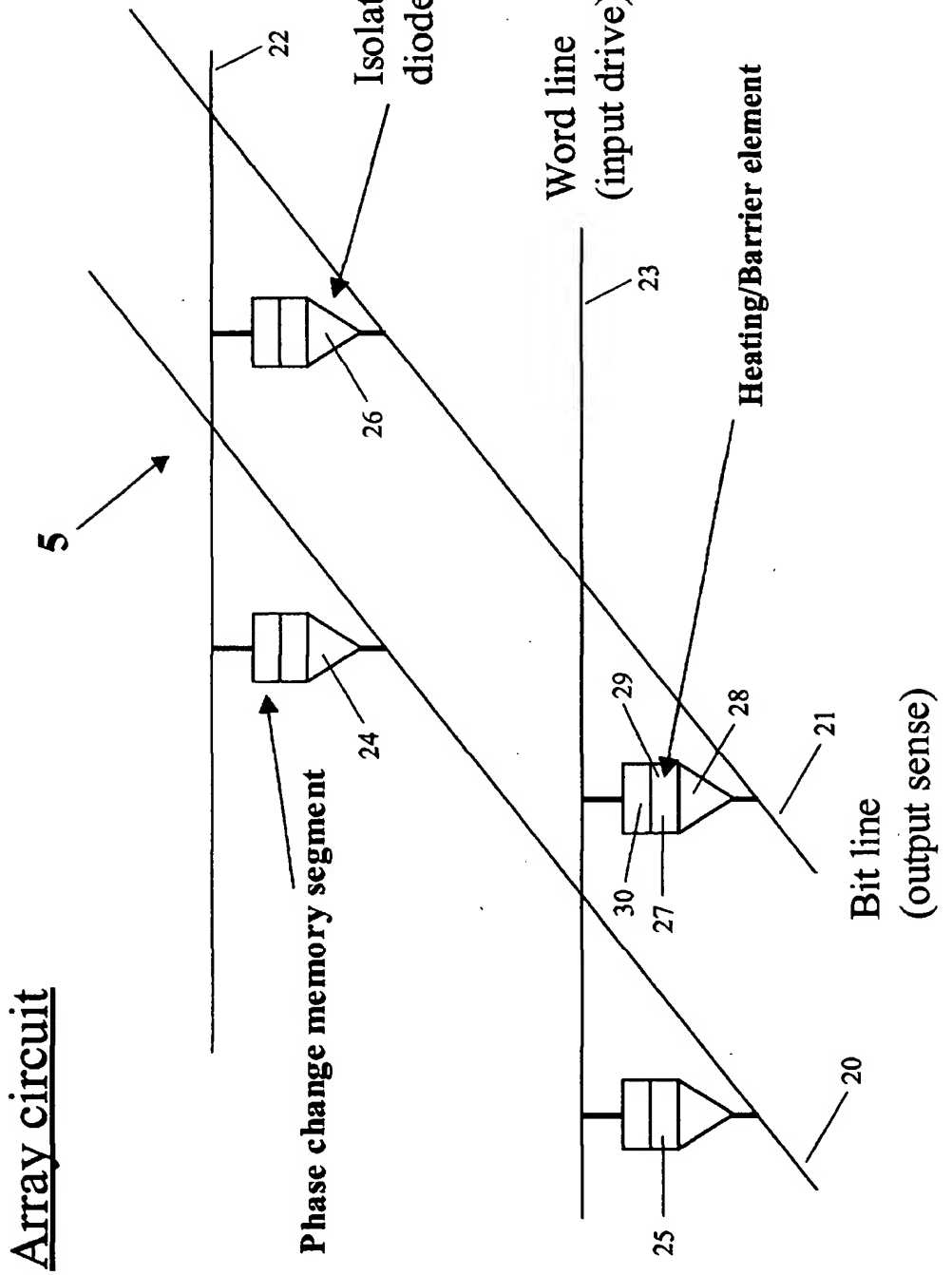

Array circuit
5
Phase change memory segment
Isolation diode
Word line (input drive)
Heating/Barrier element
Bit line (output sense)
20
21
22
23
24
25
26
27
28
29
30

Fig. 2

Fig. 3

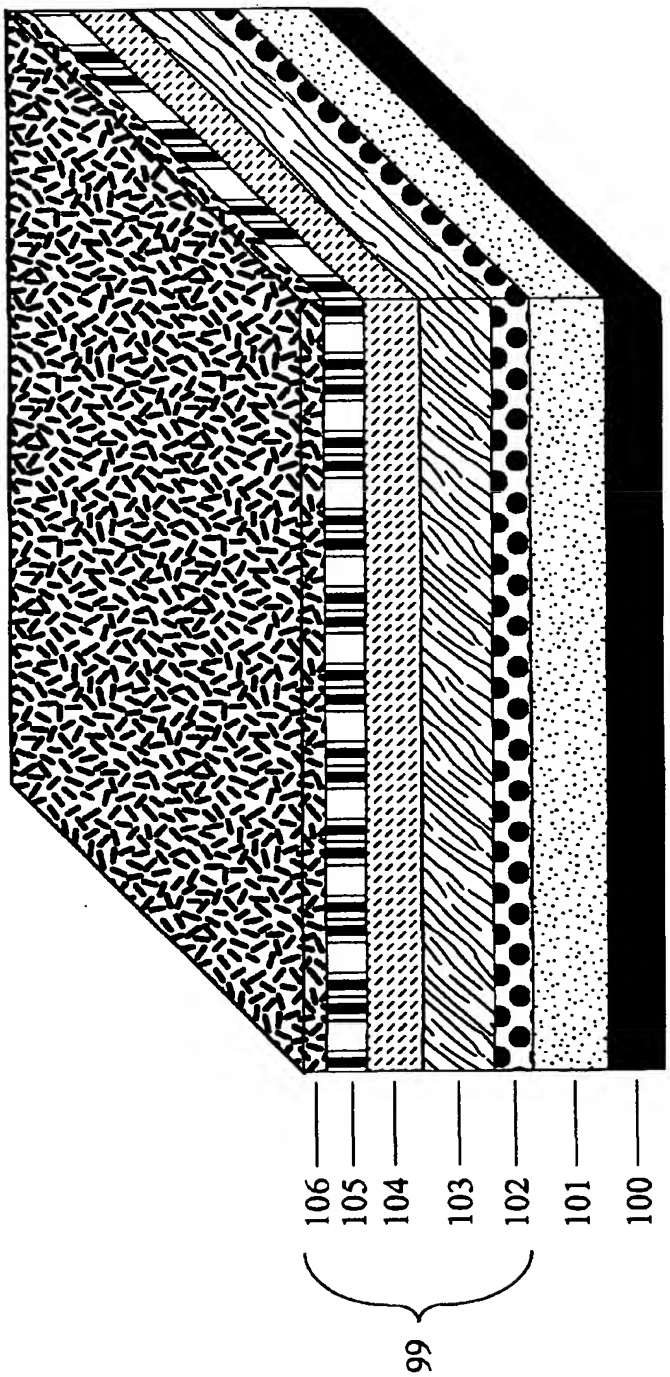


Fig. 4

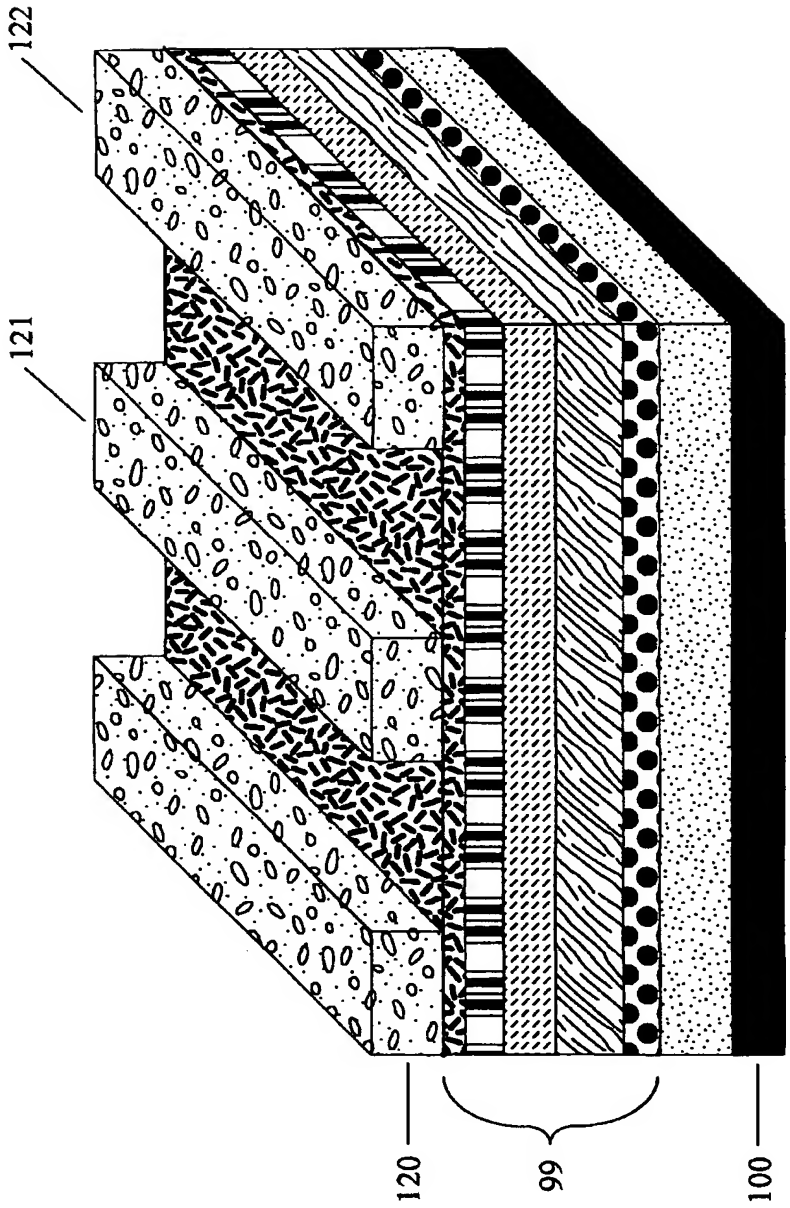


Fig. 5

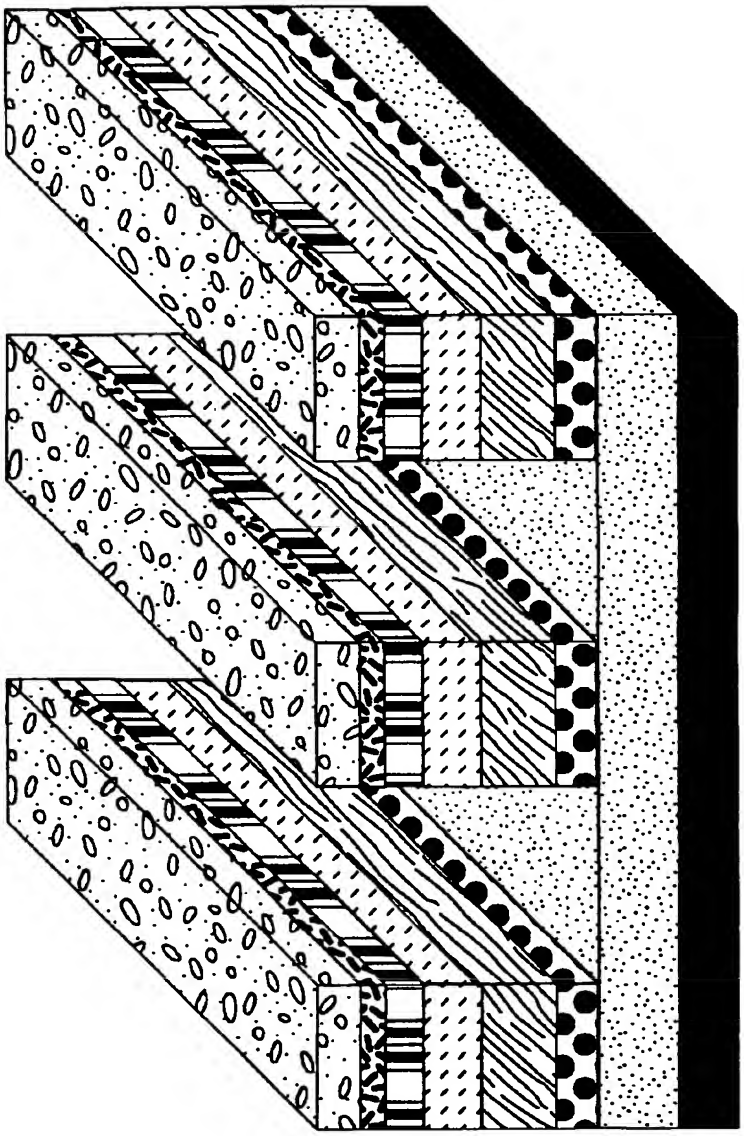


Fig. 6

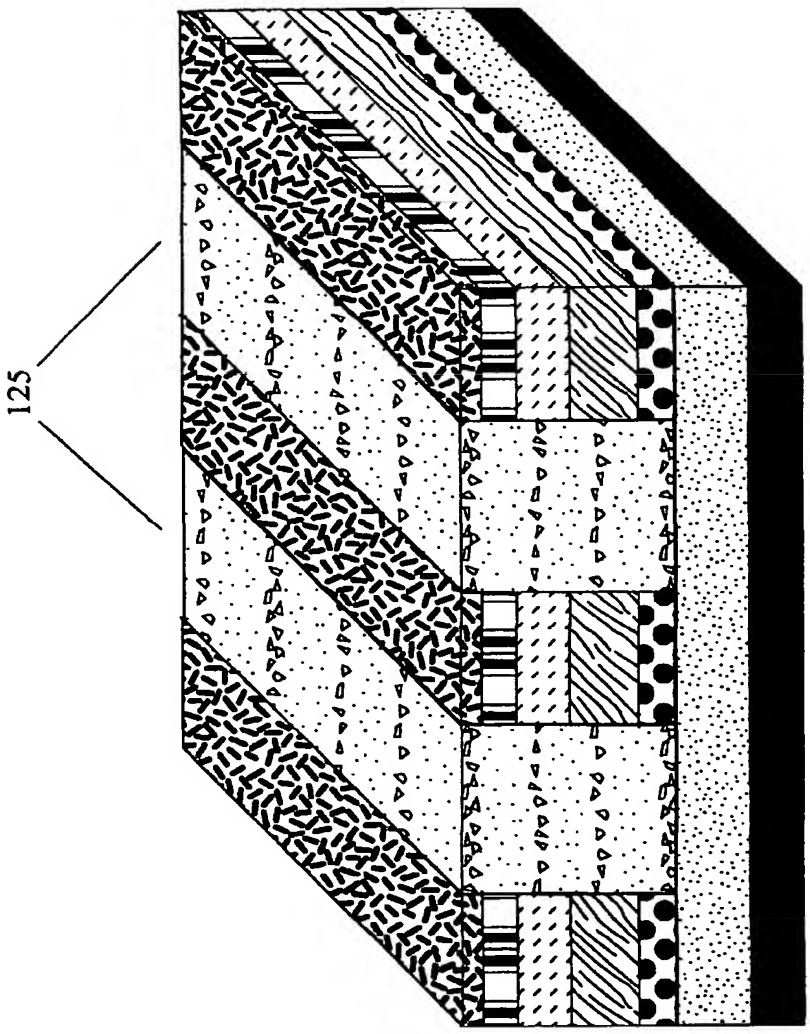


Fig. 7

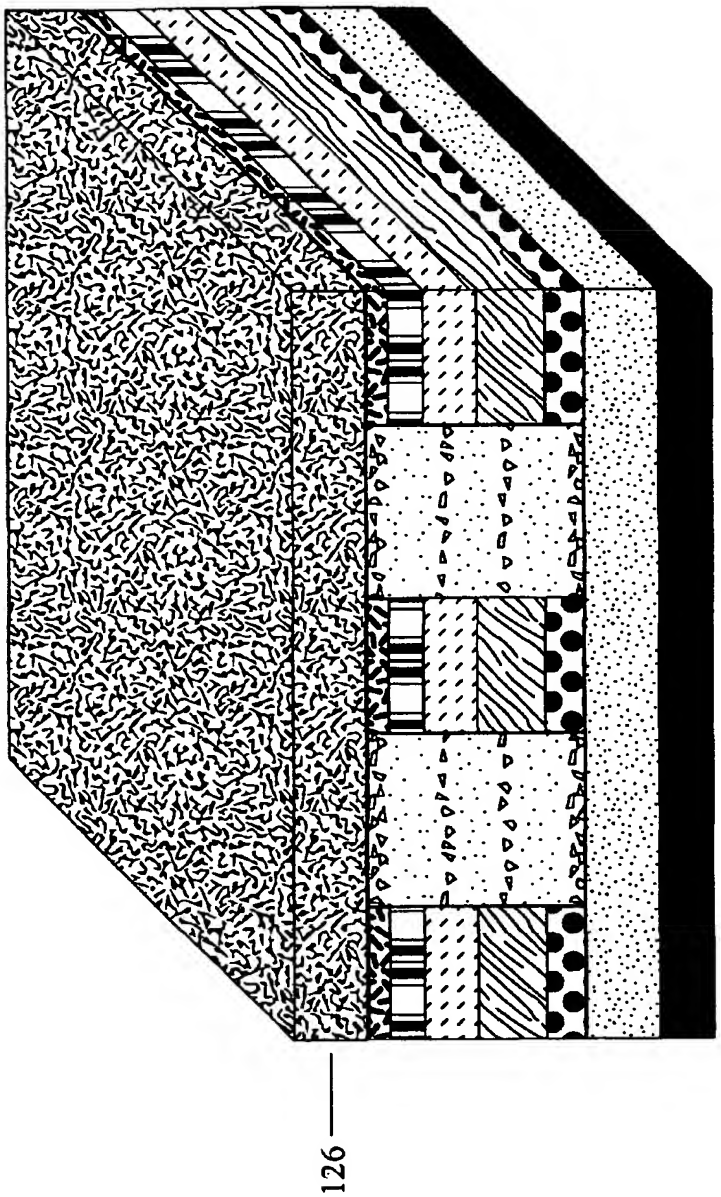


Fig. 8

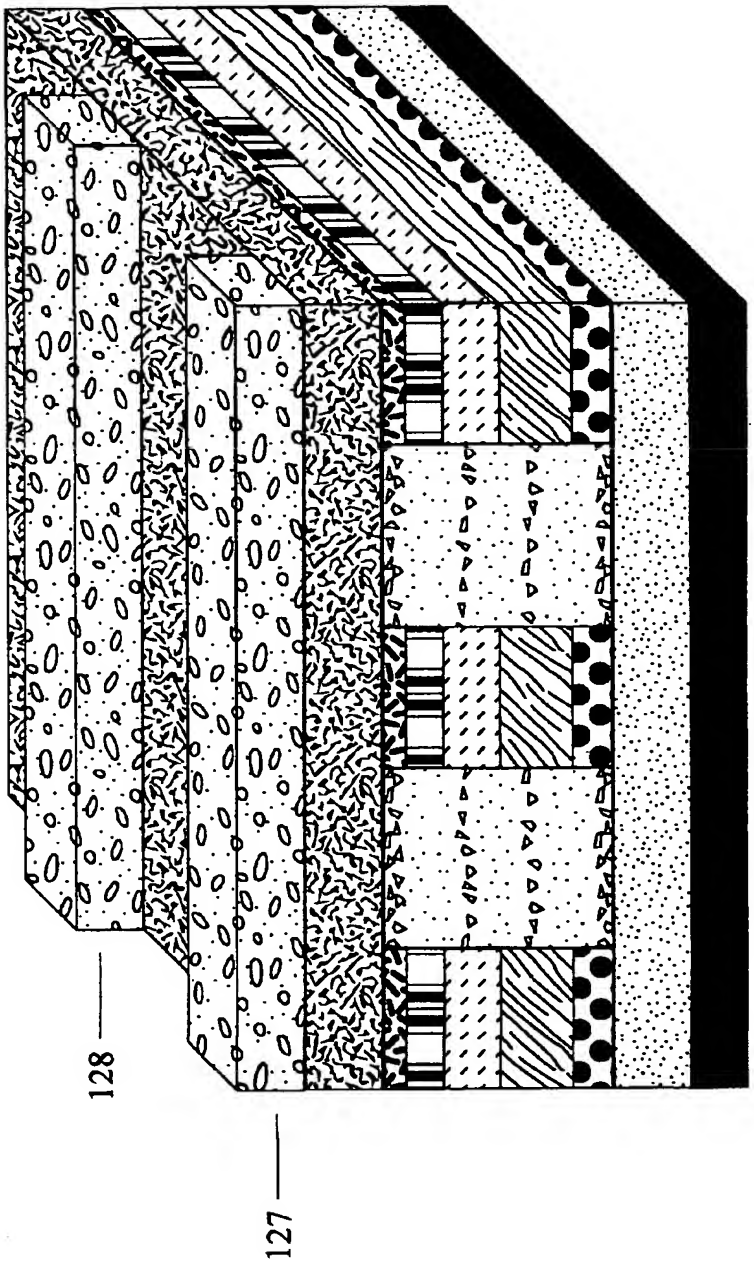


Fig. 9

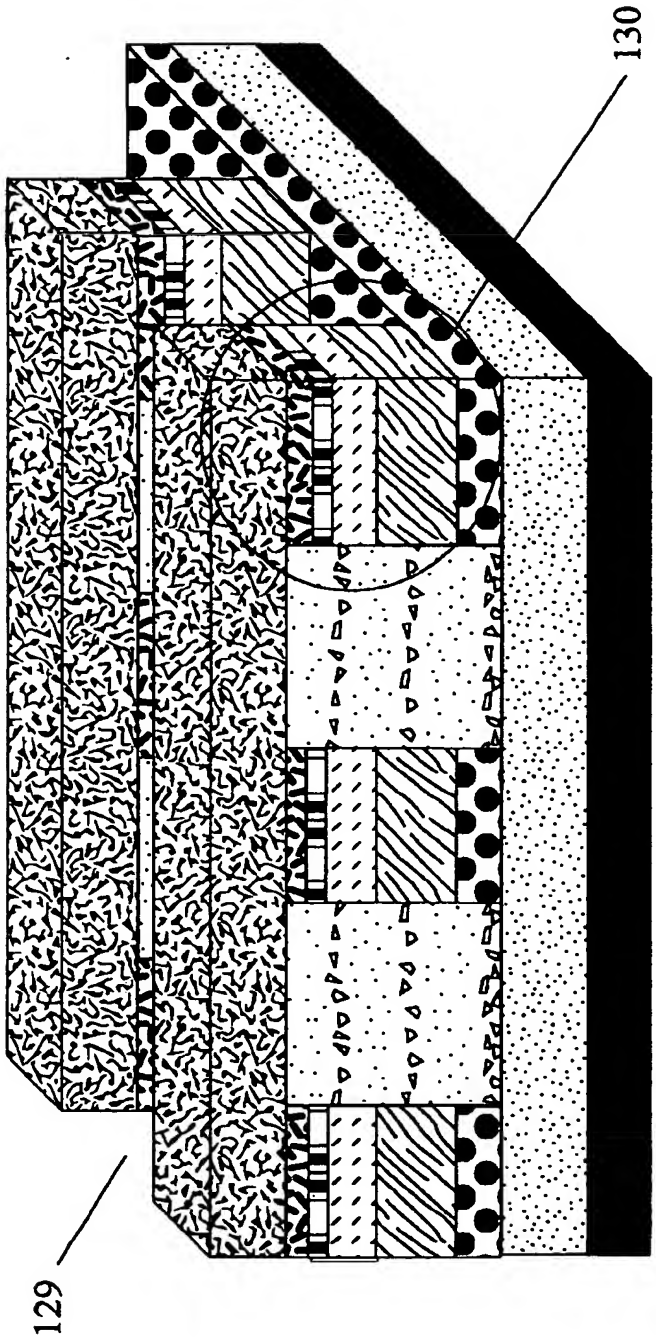
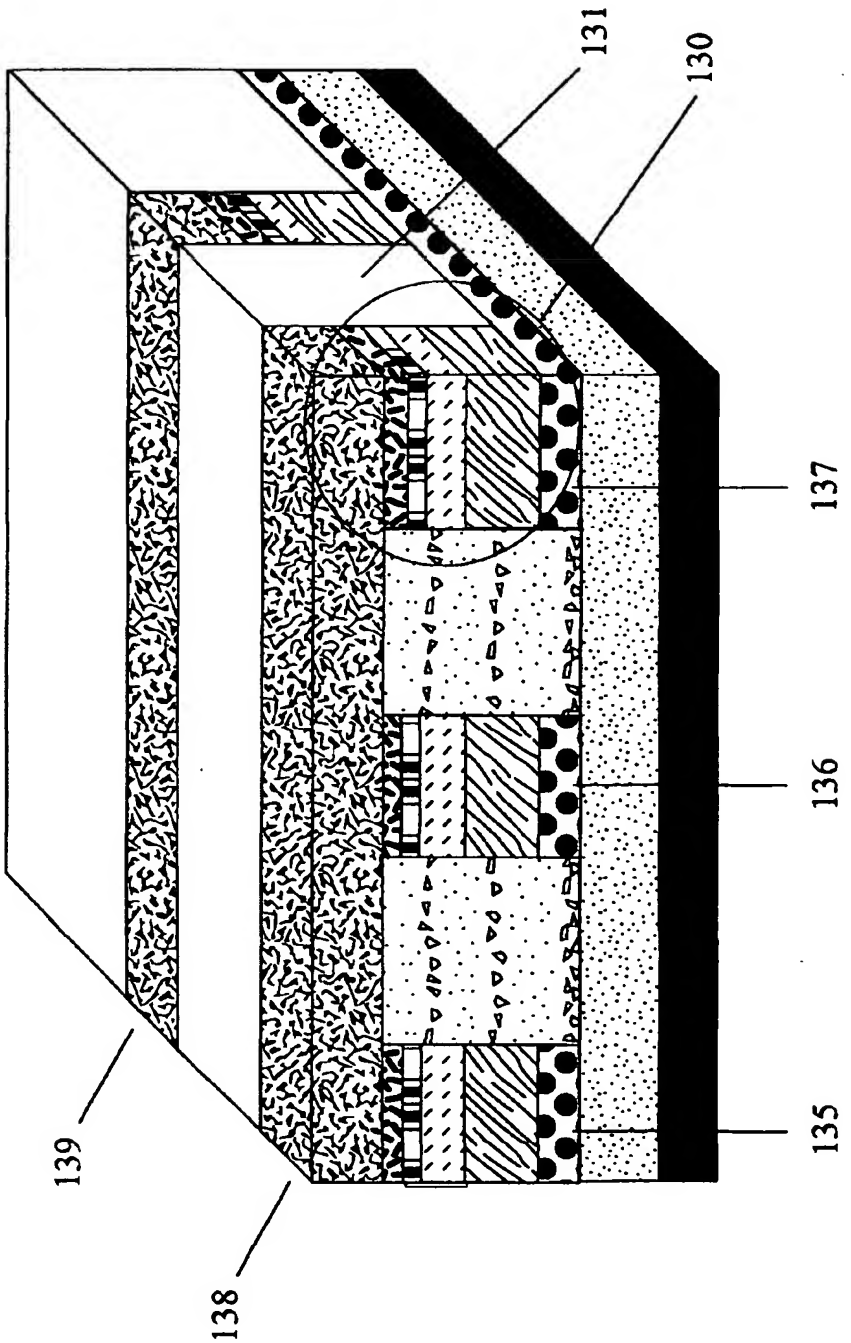


Fig. 10



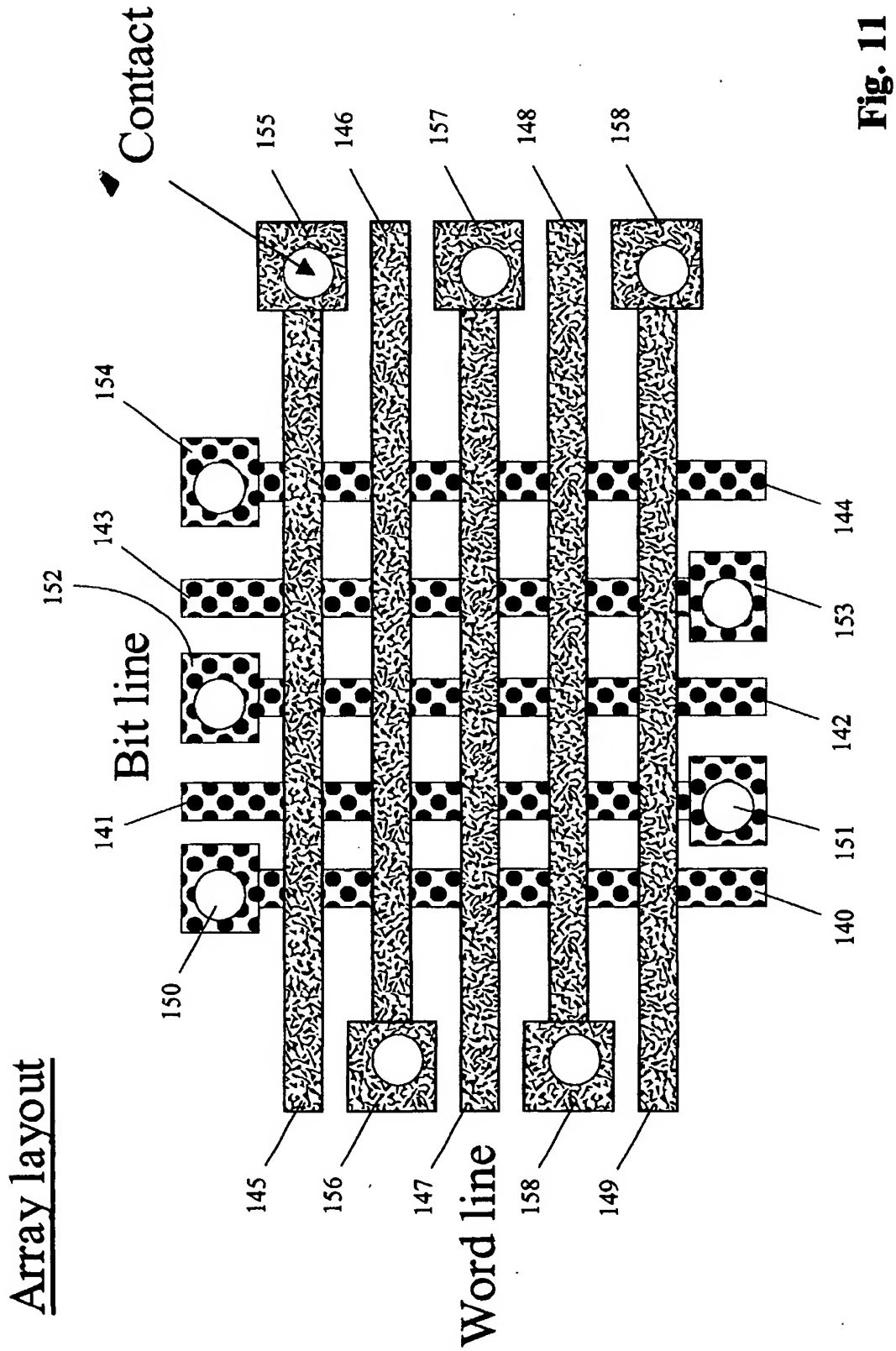

Array layout
Contact
Bit line
Word line
155
146
157
148
158
154
143
152
144
153
142
141
151
140
150
145
156
147
158
149

Fig. 11

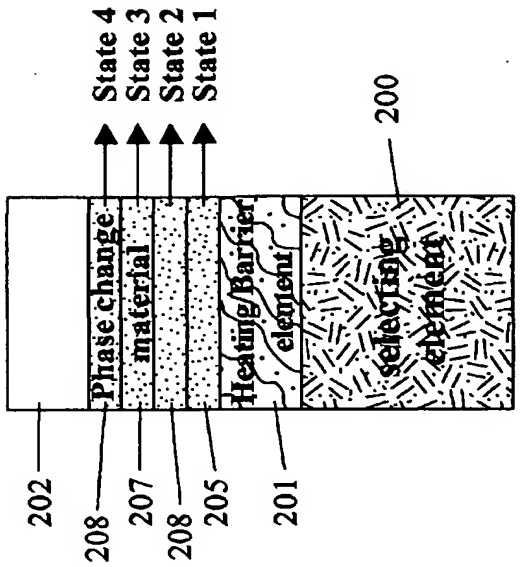


Fig. 12C

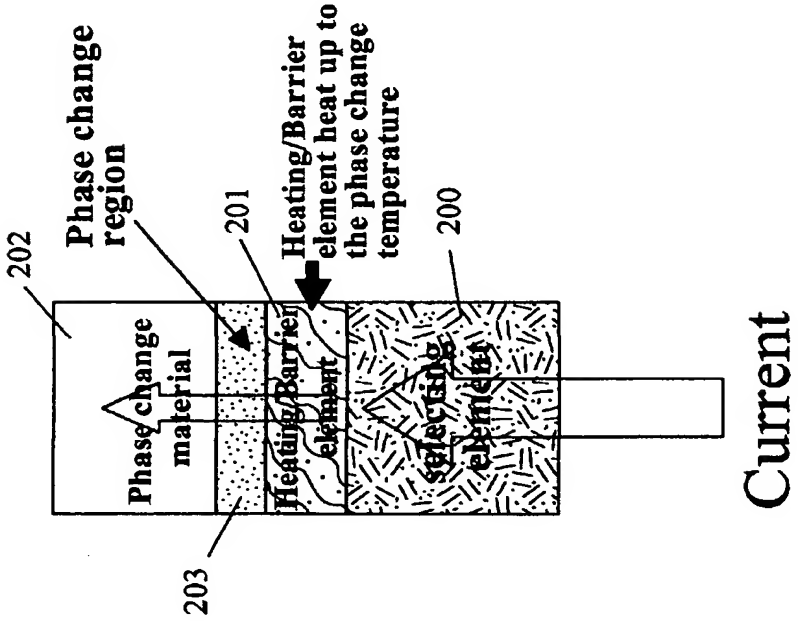


Fig. 12B

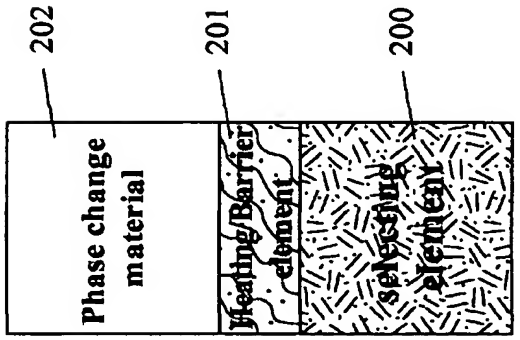


Fig. 12A

SELF-ALIGNED, PROGRAMMABLE PHASE CHANGE MEMORY

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to non-volatile, high density, integrated circuit memory devices, and more particularly to such memory devices based upon phase change material such as chalcogenides.

2. Description of Related Art

Chalcogenides have been utilized in the formation of memory cells for integrated circuit memory devices. Representative prior art patents in this field include Reinberg, U.S. Pat. No. 5,789,758; Harshfield, U.S. Pat. No. 6,077,729; Wolstenholme, et al., U.S. Pat. No. 6,153,890, Ovshinsky, U.S. Reissue Pat. No. RE37,259 (Reissue of U.S. Patent No. 5,687,112), and many others.

Chalcogenides used for integrated circuit memory devices are materials characterized by more than one solid-state phase, and which can be switched between such phases using the application of heat caused for example by electrical current or optical pulses. Memory cells which include a chalcogenide element are arranged in an array which can be addressed using conventional word lines/bit line addressing schemes common in integrated circuit memories. The state of the memory cell is determined by the bulk resistance of the chalcogenide element. Because the different solid-state phases of the chalcogenide have different resistivity, the bulk resistance of the chalcogenide element indicates the amount of the chalcogenide element in a selected phase state.

The problem of applying current at sufficient current densities to cause the phase change in the chalcogenide element is reflected in the design of the memory cells. Typically, relatively complex structures are utilized to form small pores in the current path that is coupled to the chalcogenide element. Current is concentrated through the small pores to induce a locally high current density in the chalcogenide element.

The complex structures utilized to form the pores, and other aspects of chalcogenide based memory cells, have required relatively large cell sizes to implement. Furthermore, complex structures can affect the reliability of the memory devices. Large cell sizes limit the density of the memory device, and increase its cost. Likewise, reliability in manufacturing is critical to successful commercial application of memory devices. High-density, self aligned memory cells have been manufactured for other types of storage technologies, such as the vertically stacked, non-volatile memory described in Johnson et al., U.S. Pat. No. 6,185,122. However, such high-density techniques have not been applied to phase change memory cells.

Accordingly, it is desirable to provide phase change memory cell structures and devices with smaller sizes. Furthermore, it is desirable to provide methods for manufacturing such devices, which are efficient and result in reliable structures.

SUMMARY OF THE INVENTION

The present invention provides a self-aligned, nonvolatile memory structure based upon phase change materials, including chalcogenides, and methods for manufacturing integrated circuit devices using the structure. The memory structure can be made within a very small area on an integrated circuit. For a preferred implementation, the area required for each memory cell in an array is about $4F^2$, where F is equal to the minimum line width for the manufacturing process. Thus, for processes having a minimum line width of 0.1 microns, the memory cell area is about 0.04 microns squared.

Furthermore, the manufacturing process results in self-aligned memory cells requiring only two array-related masks defining the bit lines and word lines. Memory cells are defined at intersections of bit lines and word lines, and have dimensions that are defined by the widths of the bit lines and word lines in a self-aligned process.

The use of phase change materials including chalcogenides, in the structure of the present invention provides for high-density non-volatile and programmable memory devices.

According to one embodiment of the invention, a method for manufacturing a memory device is provided. The method includes forming a multi-layer film on a surface of a substrate, where the multi-layer film includes a first conductive layer, a layer or layers of materials selected for formation of a selection device, and a layer or layers of materials selected for formation of the phase change memory element. The first array-related mask is applied to define a first plurality of lines extending in a first direction. Gaps are etched through the multi-layer film in according to the mask pattern to define the first plurality of lines. An insulating material is used to fill the gaps between the lines in the first plurality of lines.

A second conductive layer is formed over the first plurality of lines and insulating material in the gaps, to form a multi-layer composite. A second array-related mask is applied to define a second plurality of lines extending in a second direction so that the first and second pluralities of lines intersect. Gaps are etched into the multi-layer composite according to the second mask pattern to define the second plurality of lines. The gaps are etched between the second plurality of lines, and extend through the multi-layer composite to the first conductive layer, without removing the first conductor layer.

As a result of the etching steps, self-aligned stacks are formed by remaining portions of said layer or layers of materials selected for formation of a selection device, and said layer or layers of materials selected for formation of a phase change memory element. The selection device and phase change memory element in the self-aligned stacks are in electrical contact with the first plurality of lines in the first conductive layer, and the second plurality of lines remaining from the second conductive layer.

In some embodiments of the invention, the layer or layers of material selected for formation of a selection device comprise a first polysilicon layer with p-type dopant and a second polysilicon layer with n-type dopant adapted for formation of a diode.

Also, in some embodiments of the invention, the layer or layers of material selected for formation of a phase change memory element comprise a layer of chalcogenide. Further, in some embodiments, an intermediate layer is formed between the layer or layers of material selected for formation of a selection device, and the layer of phase change material. In various embodiments, the intermediate layer acts as a barrier to electromigration and diffusion of material between the materials used for the selection device, and the phase change material.

The phase change material has a first phase having a lower resistance, and a second phase having a higher resistance. Also, in various embodiments, the intermediate layer has a

resistance that is greater than the higher resistance of the phase change material in the second phase. In this way, the intermediate layer acts as a resistive heating plate to facilitate phase change in the phase change material adjacent the barrier layer.

The present invention also provides a novel memory device. The memory device comprises a substrate. A first plurality of conductive lines on the substrate extend in a first direction. A second plurality of conductive lines above the first plurality of conductive lines, extend in a second direction, and cross over the first plurality of conductive lines at intersections. A plurality of memory cells are interposed at said intersections between, and in electrical contact with, the first and second pluralities of conductive lines. The memory cells comprise self-aligned structures including a selection device and a phase change memory element, vertically arranged at the intersections.

In embodiments of the present invention, the selection device comprises a diode. The phase change memory element comprises a chalcogenide body in various embodiments. In one preferred embodiment, the chalcogenide body comprises a thin film having substantially uniform thickness across the area of the intersection.

In one embodiment, the self-aligned structure comprises a first polysilicon layer and a second polysilicon layer adapted to form the selection device, an intermediate heating/barrier plate layer, and a layer of phase change material. The intermediate layer comprises a barrier to at least one of diffusion and electromigration. In one embodiment, the intermediate layer has a first resistance, and the layer of phase change material has a first state with a first lower resistance, and a second state with a second higher resistance. The first resistance of the intermediate layer is higher than the second higher resistance of the phase change material in the second state, so that the intermediate layer acts as a heating plate facilitating phase change adjacent to barrier layer.

In various embodiments, the phase change memory element is adapted to store more than one bit by assuming more than two bulk resistance states in response to programming current or other programming stimulus.

The memory array of the present invention is formed on a substrate. In some embodiments, the substrate is an integrated circuit device having an insulating layer on the surface. The memory array is manufactured on top of insulating layer, and has contacts to the circuitry integrated into substrate. Preferably, the circuitry integrated into the substrate includes support circuitry for the memory array, including address decoders, sense amplifiers, voltage sources and alike, manufactured for example with conventional CMOS technology. In other embodiments, the circuitry integrated into the substrate may include system-on-a-chip components, including for example, a processor core and other logic.

Accordingly, the present invention provides a unique memory cell that combines polysilicon junctions and chalcogenide memory elements, and a method for manufacturing the memory device comprising the unique cells. The new memory device can be programmed and erased by applying suitable voltage and current to change the resistance of the chalcogenide memory elements. Only two array-related masks are needed to make a memory, and the resulting memory cells are fully self-aligned with the word lines and bit lines of the array. Furthermore, the area within the array for each of the resulting memory cells is only $4F^2$, where F is the minimum line width for the manufacturing process.

Other aspects and advantages of the present invention can be seen on review of the drawings, the detailed description and the claims, which follow.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a simplified block diagram of an integrated circuit memory device including self-aligned phase change cells according to the present invention.

FIG. **2** is a simplified circuit diagram of a memory array including self-aligned phase change cells according to the present invention.

FIG. **3** shows a multi-layer film on a surface of a substrate formed as an intermediate structure in manufacturing of memory cells according to the present invention.

FIG. **4** illustrates the first photoresist mask pattern for defining a first plurality of lines including bit lines in an array of memory cells according to the present invention.

FIG. **5** shows the results of etching gaps between the first plurality of lines of the mask pattern of FIG. **4**.

FIG. **6** illustrates an insulator filling the gaps between the lines of FIG. **5**.

FIG. **7** illustrates formation of a conductive layer over the structure of FIG. **6**.

FIG. **8** illustrates the second photoresist mask pattern for defining a second plurality of lines including word lines in an array of memory cells according to the present invention.

FIG. **9** shows the results of etching gaps between the second plurality of lines of the mask pattern of FIG. **8**, wherein said etching does not penetrate the bit lines.

FIG. **10** illustrates an array of memory cells manufactured according to the present invention, with an insulator filling gaps between the lines of FIG. **9**.

FIG. **11** provides a layout view of the bit lines and word lines in the structure of FIG. **10**, where self-aligned memory cells occur at intersections, and including contacts to integrated circuitry underlying the array.

FIGS. **12A–12C** schematically illustrate operation of the self-aligned memory cells in single bit and multibit applications.

DETAILED DESCRIPTION

A detailed description of embodiments of the present invention is provided with reference to FIGS. **1** through **12A–12C**. FIG. **1** is a block diagram of an integrated circuit memory device including a memory array **5** comprising self-aligned phase change cells according to the present invention. The integrated circuit includes a substrate in which circuitry supporting the memory array is disposed. The circuitry includes address decoders, input drivers, and output drivers in this example. Thus, y-decoder and input driver circuitry **10** and **11** are disposed next to the array. Also, x-decoder and output sense amplifier circuitry **12** and **13** are disposed next to the array. In one embodiment, a program and erase voltage generator circuit **14** is included on the integrated circuit. Such a voltage generator circuit **14** may include charge pumps or other high voltage or negative voltage generators as required for programming and erasing the phase change cells.

In one embodiment, the integrated circuitry is implemented using standard CMOS techniques. Other manufacturing techniques, including advanced materials and processes may be used for the circuitry integrated in the substrate. In addition, the layout of the circuitry may include logic control circuit beneath the array **5**.

FIG. 2 shows a basic circuit layout for the array 5 of self aligned phase change memory cells according to the present invention. The array 5 includes bit lines 20 and 21, and word lines 22 and 23, which are arranged so that they intersect at memory cells 24–27. The memory cells 24–27 are disposed at the intersections between the bit lines and the word lines. The memory cells, for example memory cell 27, include a selection device 28, a heating/barrier layer 29 and a phase change layer 30. A selection device 28 comprises an isolation diode in one embodiment. The phase change layer 30 comprises the chalcogenide memory element in a preferred embodiment. A memory cell is selected by biasing the word line and bit line which intersect at the selected memory cell, so that the isolation diode of the selection device is conductive, while word lines and bit lines coupled to other memory cells are reverse biased so that the isolation diode of the selection device is nonconductive. As shown in FIG. 2, the bit lines 20, 21 are coupled to output sense amplifier circuitry. The word lines 22, 23 are coupled to input drivers.

A method for manufacture of the memory array, and the structure of the memory cells, of a preferred embodiment of the present invention are described with reference to FIGS. 3-10.

FIG. 3 illustrates a multilayer film 99 formed on a substrate 100. The substrate 100 comprises a semiconductor having circuitry integrated therein as discussed above. The substrate 100 includes an insulator 101 on the surface. The insulator in this embodiment comprises silicon dioxide. The material and thickness of the insulator 101 are chosen so that the memory array is isolated from the underlying integrated circuitry. The multilayer film 99 includes a layer 102 of bit line material, a first polysilicon layer 103, a second polysilicon layer 104, an intermediate heating/barrier layer 105 and a layer 106 of chalcogenide.

The layer 102 of bit line material comprises tungsten in this embodiment between 150 and 600 nanometers thick, deposited using chemical vapor deposition. A variety of other materials are suitable for use as the bit line material, for example heavily doped polysilicon, or other high melting point metals or compounds, such as Ta, Pt, TiN, TaN, WSi and alloys thereof, are possible.

The first polysilicon layer 103 comprises n- doped polysilicon 100 to 600 nanometers thick deposited using CVD, plasma enhanced CVD or sputtering, and doped using a n-type donor such as arsenic or phosphorus. The second polysilicon layer 104 comprises p+ doped polysilicon about 100 to 400 nanometers thick deposited using CVD, plasma enhanced CVD or sputtering, and doped using a p-type donor such as B, Ga, or Indium. The first and second layers of polysilicon are adapted to form a selection device in the form of the diode. The layers of materials chosen to implement the selection device can implement junctions other than p+/n–junctions. Other types of junctions such as n+/p–, p+/intrinsic/n–, n+/intrinsic/p–, p+/n+, p+/intrisic/n+and Schottky junctions are possible. Also other selection device structures may be used.

The intermediate heating/barrier layer 105 in this embodiment comprises a film of material 20 to 200 nanometers thick deposited for example by sputtering or CVD. In the preferred embodiment, the intermediate layer acts as a heating element to heat up phase change material and a barrier to electromigration and diffusion. In addition, the material of the intermediate layer does not react with the phase change material and the selection element. In the preferred system, the resistance of the intermediate layer is higher than the resistance of the phase change material in a high resistance phase. In this manner, it can act as a heating plate to facilitate changing phase of the phase change material adjacent to the barrier layer. Suitable materials include TiW, TiAlN, Ta, Mo and others. A variety of other materials characterized by relatively high resistance, compared to the high resistivity phase of the phase change material, and good barrier characteristics can be utilized. The intermediate layer 105 can be chosen from a compound which includes one element selected from the group consisting of Ti, V, Cr, Zr, Nb, M, Hf, Ta, W and two or more elements selected from the group B, C, N, Al, Si, P and S. Candidate barrier materials are described in U.S. Reissue Patent No. RE37,259 at column 13, line 31 through column 14, line 4. The intermediate layer 105 in various embodiments may include one material chosen for barrier characteristics and another material chosen for suitability as heating plate. Preferably, a single material performs both functions.

The top layer in the multilayer film shown in FIG. 3 is the phase change material. In this example, the phase change material comprises a film of chalcogenide. In some embodiments, thin films of materials chosen to act as top or bottom electrodes for the chalcogenide layer can be included. Although chalcogenide is utilized in this embodiment, all kinds of phase change materials can be used. The chalcogenide material in this example is about 5 to 200 nanometers thick, and preferably between 20 and 40 nanometers thick. Typically chalcogenide materials are deposited using sputtering. Representative phase change materials include chalcogenides such as those described in U.S. Reissue Patent No. RE37,259.

After formation of the multilayer film shown in FIG. 3, the next step in the manufacturing process is shown in FIG. 4. This next step is used for defining a first plurality of lines using photoresist having a first mask pattern as shown in FIG. 4. Thus, lines 120, 121, 122 are defined using photoresist. The lines 120, 121, 122 are substantially parallel and extend in a first direction, and are used to define the bit lines for the array.

FIG. 5 illustrates gaps etched, using reactive ion etching, into the multilayer film using the mask shown in FIG. 4. The etching of the gaps is stopped at the insulator layer 101, and defines bit lines in the bit line layer 102. As shown in FIG. 6, the gaps are filled with an oxide 125 or other good insulation material, using a high-density plasma chemical vapor deposition process, or other process suitable for filling narrow gaps.

FIG. 7 illustrates a next step in the process of manufacturing them every array. In the step, a word line conductor layer 126 is deposited over the lines and oxide 125 of the structure shown in FIG. 6. The word line conductor layer 126 comprises a conductive material such as W, Ta, Pt, TiN, TaN, WSi or heavily doped polysilicon. Such materials may be deposited for example by sputtering or chemical vapor deposition.

FIG. 8 illustrates a second plurality of lines defined by a second mask step resulting in photoresist lines 127, 128 as shown. The second plurality of lines extended a second direction generally orthogonal to the direction of the bit lines.

FIG. 9 shows the structure resulting from a reactive ion etching of the gaps (e.g. gap 129) between the second plurality of lines in the structure of FIG. 8. The etching is stopped on the bit line layer. As a result of the second etching step, memory cells (e.g. cell 130) are disposed between the word lines and a bit lines at the intersections. The word lines

and the bit lines lie in essentially parallel planes, but intersect in the plan view of the array. The memory cells are self-aligned with the word lines and bit lines, because the sides of the cells are defined using the same mask steps as are used to define the word lines and the bit lines. As shown in FIG. **10**, a final step in formation of the memory array is the filling of the gaps in the structure of FIG. **9** with an insulator **131** using any high-density plasma chemical vapor deposition of oxide or other suitable insulator.

The basic structure of the memory array is shown in FIG. **10**. The array includes a first plurality of conductive lines **135, 136, 137** and a second plurality of conductive lines **138, 139**. The second plurality of conductive lines **138, 139** crosses over the first plurality of conductive lines at intersections. Memory cells, for example memory cell **130**, are disposed at the intersections, and are in series electrical contact with the first and second pluralities of conductive lines. The memory cells comprise self-aligned structures including a selection device formed from remaining portions of the first and second polysilicon layers, an intermediate heating/barrier plate layer and a chalcogenide element, all arranged vertically at intersections between the first and second pluralities of conductive lines.

A layout plan view of the array can be seen with reference to FIG. **11**. Thus, bit lines **140–144** are arranged vertically in the array shown in FIG. **11**. Word lines **145–149** are arranged horizontally in the array. The bit lines **140–144** extend to respective contact structures **150–155**. Likewise the word lines **145–149** extend to respective contact structures **155–159**. The contact structures comprise for example tungsten plugs extending through the insulator layer **101** to the circuitry integrated in the substrate.

Operation of the memory cells of the present invention is described with reference to FIGS. **12A–12C**. FIG. **12A** illustrates the basic memory cell of the present invention including a selecting element **200**, a barrier/heating plate layer **201**, and a phase change element **202**. As shown in FIG. **12B**, when current is applied the barrier/heating plate layer **201** heats up to the phase change temperature of the phase change element **202**. The phase change element comprises material having a first solid-state phase with a lower resistance, and a second solid-state phase with a higher resistance. Material of the phase change element **202** in the region **203** adjacent to barrier/heating plate layer **201** changes phase. The bulk resistance of the phase change element **202** indicates the relative amounts of material of the phase change element in first and second solid-state phases. By controlling the phase change, data is stored in the phase change element **202**.

FIG. **12C** illustrates a multibit embodiment, including a selecting element **200**, a barrier/heating plate element **201**, and a phase change element **202**. In this embodiment, the phase change is controlled so that more than 2 memory states are achieved. Thus for example, in state **1** the material in region **205** is in the high resistance state. In state **2**, the material in regions **205** and **206** is in the high resistance state. In state **3**, the material in regions **205, 206** and **207** is in the high resistance state. In state **4**, the material in regions **205, 206, 207**, and **208** are all in the high resistance state. So, in this example, there are four different resistance states stored in a cell, and the four different states can represent 2 bits in one cell.

Basic operation of the device can be understood with reference to FIG. **10**. The top metal lines act as word lines, and the bottom metal lines act as bit lines. The p+/n− polysilicon junction acts as a diode to isolate/select each memory cell. When programming or erasing a cell, a suitable voltage is built between the word lines and bit lines to supply enough current penetrating the chalcogenide and barrier/heating plate layer to generate heat. By controlling the heating rate, the solid-state phase of the chalcogenide is controlled to establish a memory state indicated by the bulk resistance of the chalcogenide. When reading the cell, a current flows from the word lines through the chalcogenide, barrier/heating plate layer and p+/n− junction to the bit line. By distinguishing the voltage or current level of the specific cell, the data is sensed.

The memory array of the present invention can be used for one-time programmable non-volatile memory, non-volatile memory programmed during manufacture, and electrically erasable and programmable random access memory suitable for thousands of program and erase cycles.

While the present invention is disclosed by reference to the preferred embodiments and examples detailed above, it is to be understood that these examples are intended in an illustrative rather than in a limiting sense. It is contemplated that modifications and combinations will readily occur to those skilled in the art, which modifications and combinations will be within the spirit of the invention and the scope of the following claims.

What is claimed is:

1. A memory device, comprising:

a substrate;

a first plurality of conductive lines on the substrate extending in a first direction;

a second plurality of conductive lines above the first plurality of conductive lines, and extending in second direction and crossing over the first plurality of conductive lines at intersections;

a plurality of memory cells at said intersections and in electrical contact with the first and second pluralities of conductive lines, the memory cells comprising self-aligned structures including a selection device, and a phase change memory element.

2. The memory device of claim **1**, wherein said memory cells comprise respective multi-layer stacks including a layer or layers of material adapted to act as said selection device, and a layer or layers of material selected for formation of a heating/barrier element, and a layer or layers of material adapted to act as said phase change memory element.

3. The memory device of claim **1**, wherein said phase change memory elements comprise respective chalcogenide bodies.

4. The memory device of claim **3**, wherein said chalcogenide bodies comprise respective films having substantially uniform thickness across said intersections.

5. The memory device of claim **1**, wherein said memory cells comprise respective multi-layer stacks including a layer or layers of material adapted to act as said selection device, and an intermediate layer of material having a first resistance and a layer of phase change material adjacent the intermediate layer, and having a first phase having a lower resistance and a second phase having a higher resistance, wherein the first resistance is greater than the higher resistance of the phase change material in the second phase.

6. The memory device of claim **5**, wherein said intermediate layer comprises a barrier to at least one of diffusion and electromigration.

7. The memory device of claim **5**, wherein said layer or layers of material adapted to act as a selection device, comprise a first polysilicon layer with p-type dopant and a

second polysilicon layer with n-type dopant adapted for formation of a diode.

8. The memory device of claim 1, wherein said memory cells comprise respective multi-layer stacks including a layer or layers of material adapted to act as said selection device, and a layer or layers of material selected for formation of a heating/barrier element, and a layer or layers of material adapted to act as said phase change memory element, wherein said layer or layers of material adapted to act as said phase change memory element comprise a layer of chalcogenide.

9. The memory device of claim 8, wherein said layer of chalcogenide overlays said layer or layers of material selected for formation of a selection device.

10. The memory device of claim 8, wherein said layer or layers of material adapted to act as a selection device, comprise a first polysilicon layer with p-type dopant and a second polysilicon layer with n-type dopant adapted for formation of a diode.

11. The memory device of claim 1 wherein said substrate includes an insulator at said surface.

12. The memory device of claim 1, wherein said substrate comprises an integrated circuit device, with an insulator at said surface.

13. The memory device of claim 1, wherein said phase change memory element is adapted to store more than one bit by assuming more than two bulk resistance states in response to programming current.

14. A memory device, comprising:

a substrate having a surface, including integrated circuitry and an insulation layer on the surface;

a first plurality of conductive lines on the insulation layer on the surface of the substrate extending in a first direction, and contacting said integrated circuitry at contact points;

a second plurality of conductive lines above the first plurality of conductive lines, and extending in second direction and crossing over the first plurality of conductive lines at intersections, and contacting said integrated circuitry at contact points;

a plurality of memory cells at said intersections and in electrical contact with the first and second pluralities of conductive lines, the memory cells comprising self-aligned structures including a selection device, an intermediate layer and a chalcogenide memory element.

15. The memory device of claim 14, wherein said chalcogenide memory elements comprise respective chalcogenide films having substantially uniform thickness across said intersections.

16. The memory device of claim 14, wherein said intermediate layer has a first resistance and said chalcogenide memory element comprises a chalcogenide material having a first phase having a lower resistance and a second phase having a higher resistance, wherein the first resistance is greater than the higher resistance of the chalcogenide material in the second phase.

17. The memory device of claim 14, wherein the intermediate layer comprises a heating element.

18. The memory device of claim 14, wherein the intermediate layer comprises a barrier to at least one of diffusion and electromigration.

19. The memory device of claim 14, wherein said selection devices comprise a first polysilicon layer with p-type dopant and a second polysilicon layer with n-type dopant adapted for formation of a diode.

20. The memory device of claim 14, wherein said chalcogenide memory element is adapted to store more than one bit by assuming more than two bulk resistance states in response to programming current.

* * * * *

37 CFR 1.501
US 7,034,332

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United States Patent [19]

Chou

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[54] **NANOIMPRINT LITHOGRAPHY**

[75] Inventor: **Stephen Y. Chou**, Golden Valley, Minn.

[73] Assignee: **Regents of the University of Minnesota**, Minneapolis, Minn.

[21] Appl. No.: **558,809**

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[51] **Int. Cl.**[6] **H01L 21/304**

[52] **U.S. Cl.** **216/44**; 216/52; 216/53; 438/691; 438/700; 438/735

[58] **Field of Search** 216/11, 40, 44, 216/52, 53, 58, 83; 438/691, 700, 735

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Primary Examiner—R. Bruce Breneman
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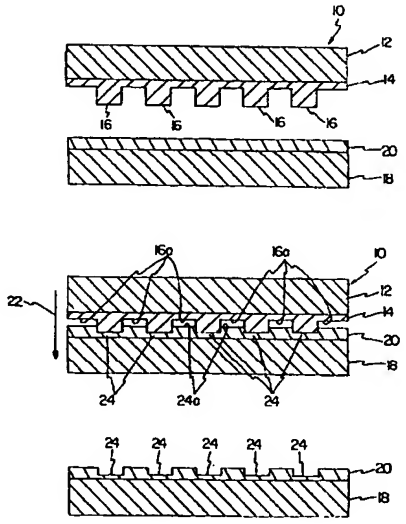
Attorney, Agent, or Firm—Westman, Champlin & Kelly, P.A.

[57] **ABSTRACT**

A lithographic method and apparatus for creating ultra-fine (sub-25 nm) patterns in a thin film coated on a substrate is provided, in which a mold having at least one protruding feature is pressed into a thin film carried on a substrate. The protruding feature in the mold creates a recess of the thin film. The mold is removed from the film. The thin film then is processed such that the thin film in the recess is removed exposing the underlying substrate. Thus, the patterns in the mold is replaced in the thin film, completing the lithography. The patterns in the thin film will be, in subsequent processes, reproduced in the substrate or in another material which is added onto the substrate.

19 Claims, 9 Drawing Sheets



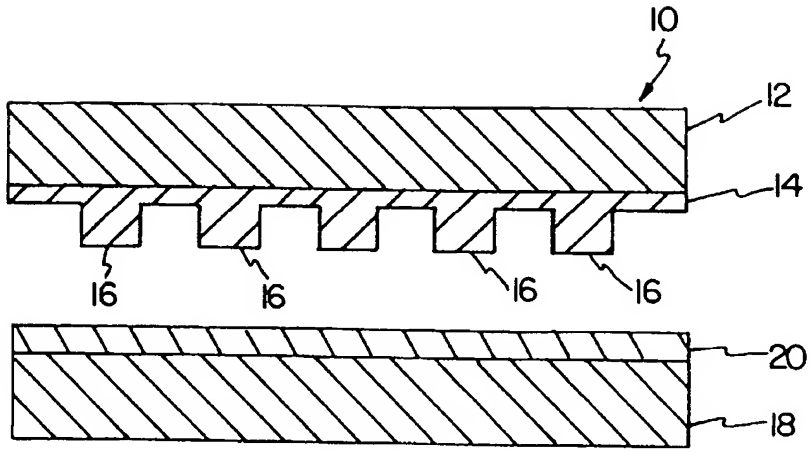


Fig. 1A

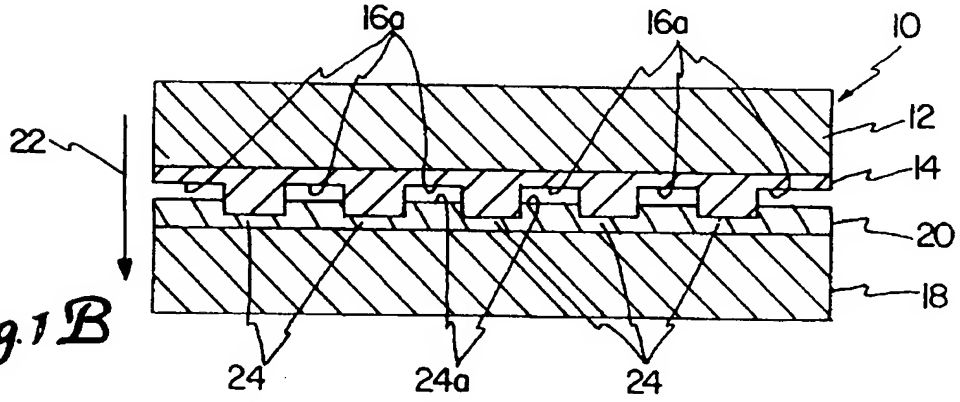


Fig. 1B

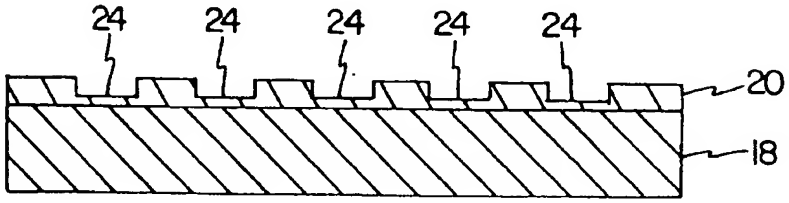


Fig. 1C

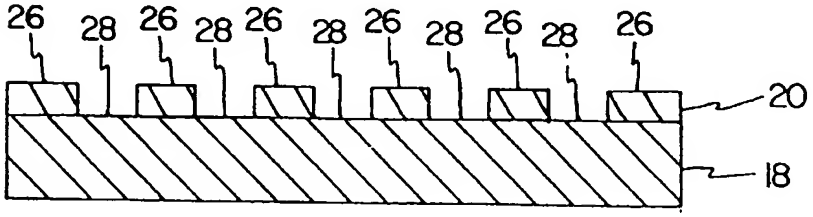


Fig. 1D

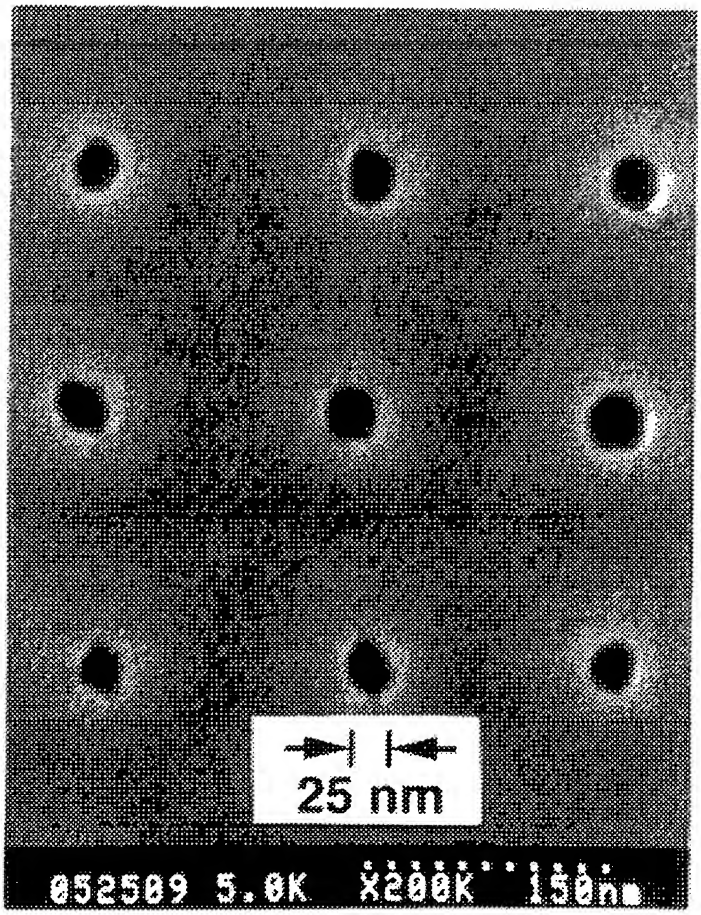


Fig. 2

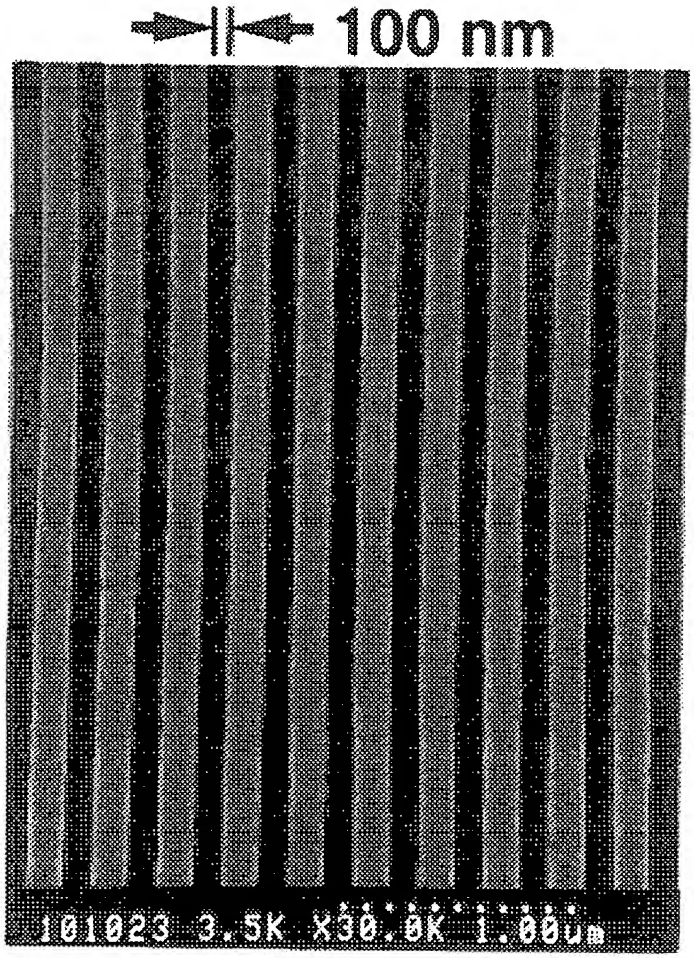


Fig. 3

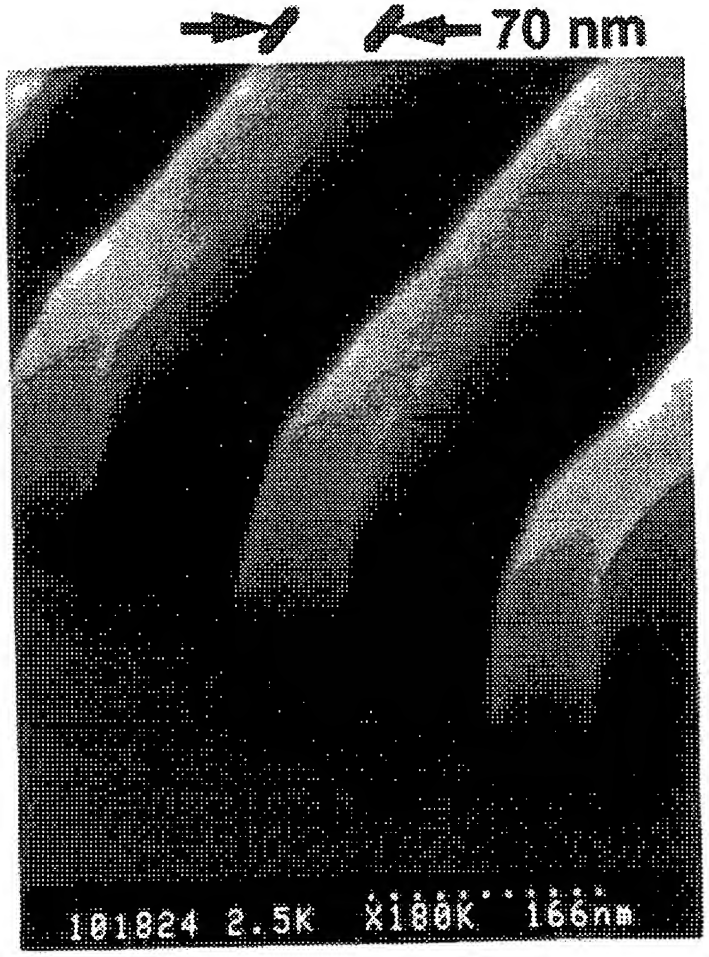


Fig. 4

Fig. 5A

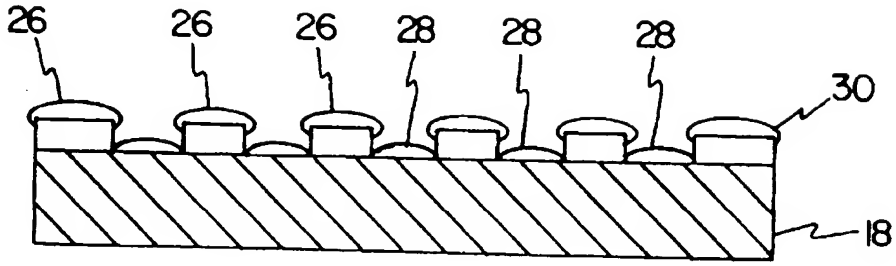
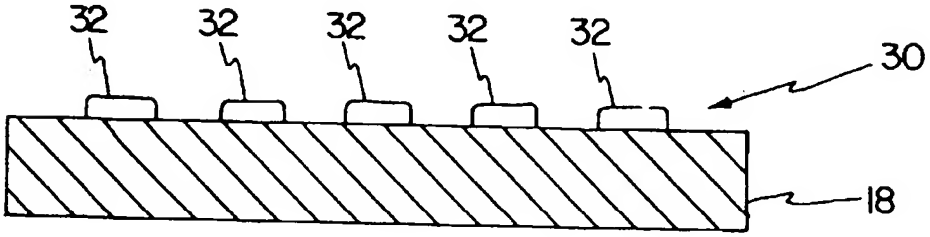


Fig. 5B



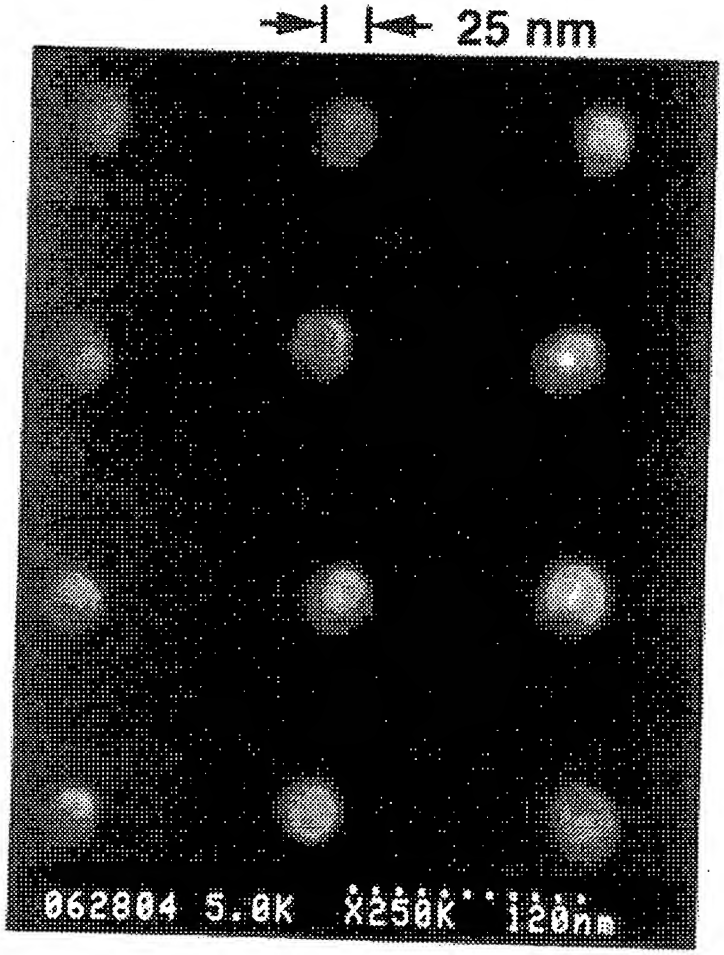


Fig. 6

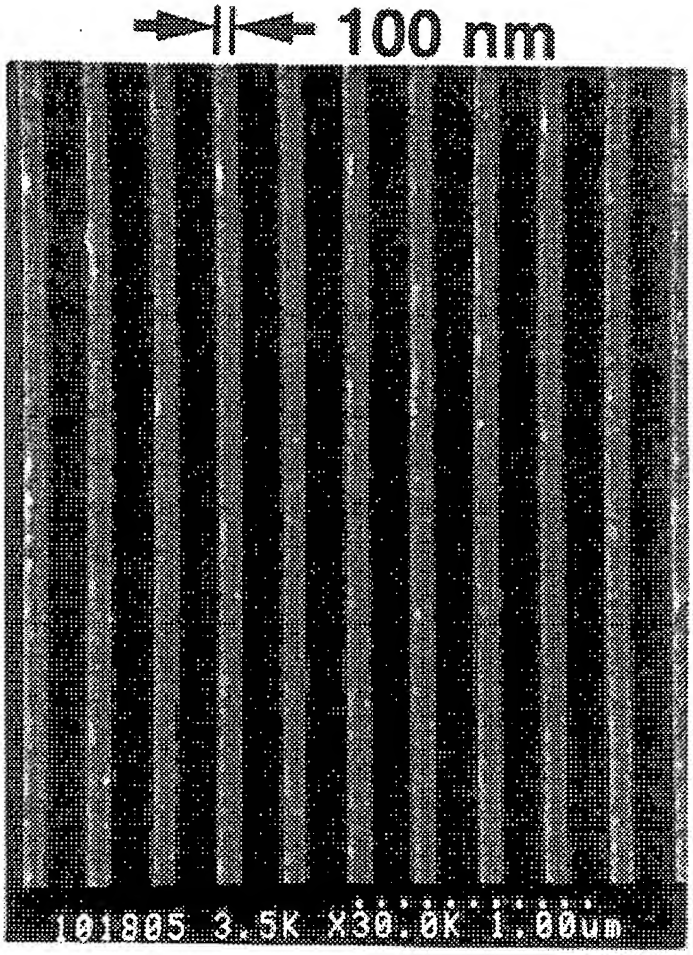


Fig. 7

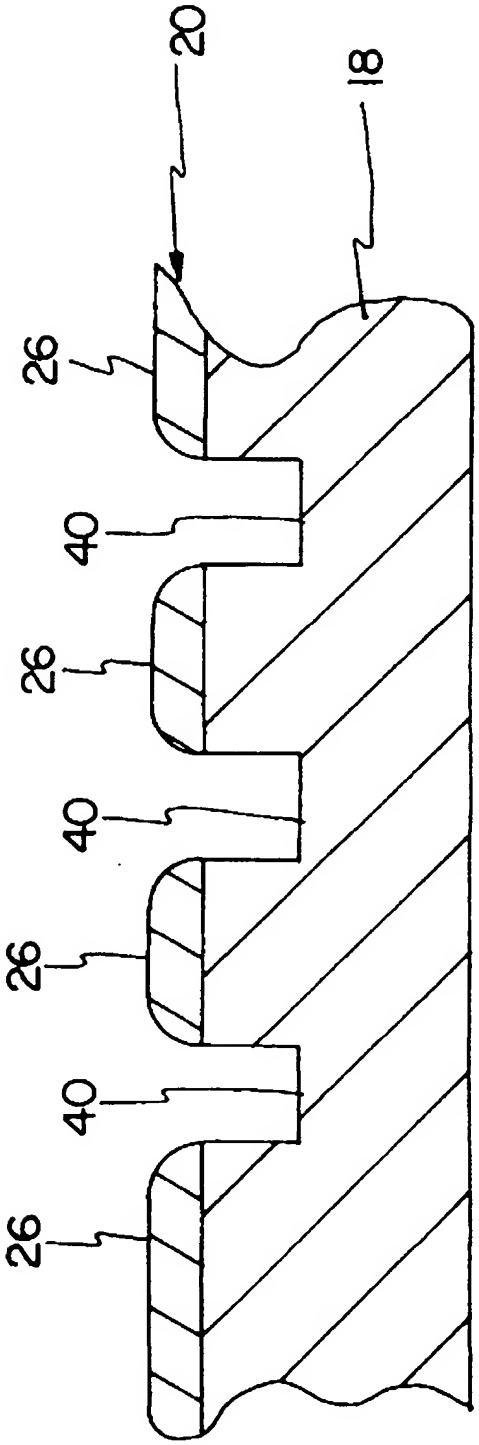


Fig. 8

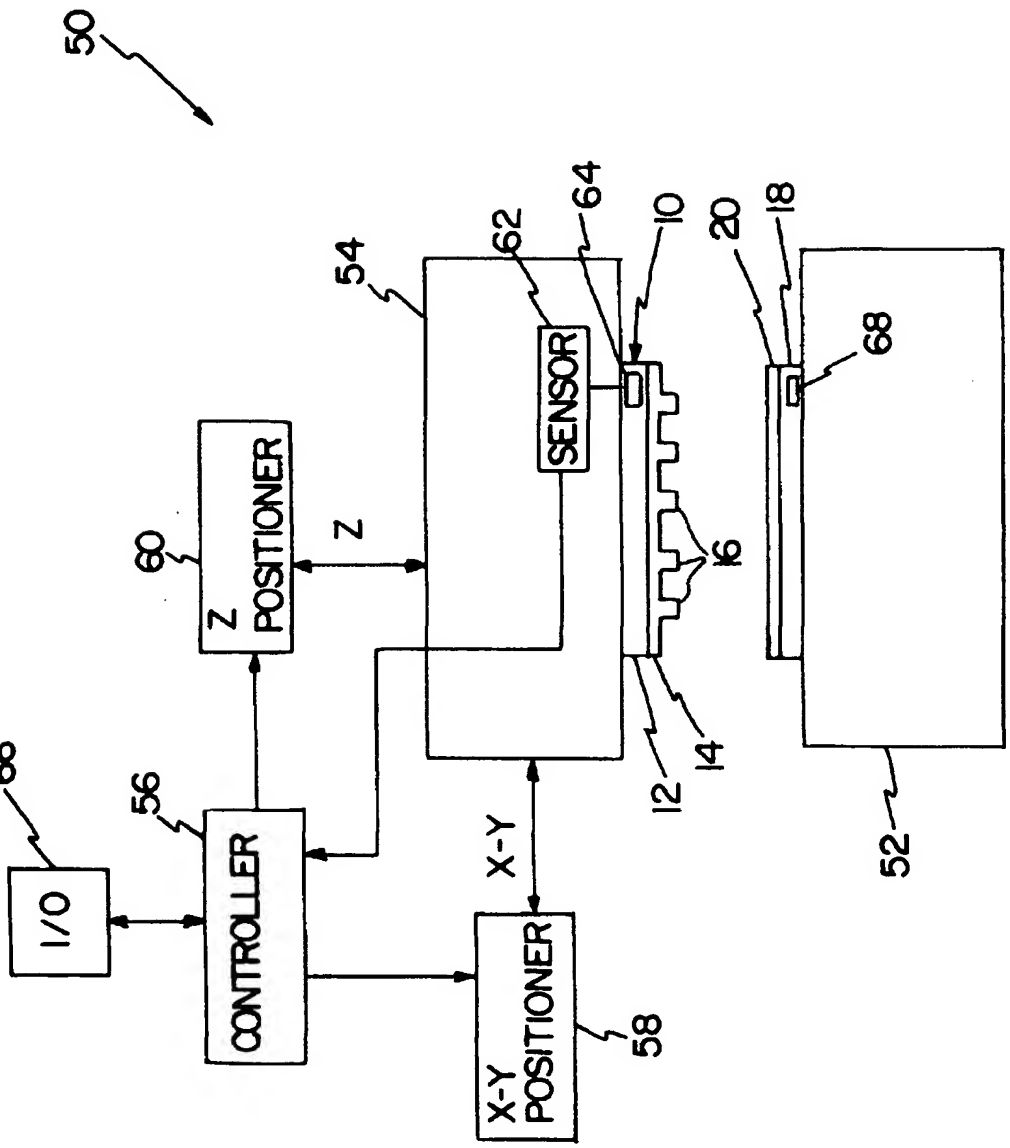

50
54
62
64
10
20
18
68
SENSOR
Z POSITIONER
60
Z
16
66
56
I/O
CONTROLLER
X-Y
X-Y POSITIONER
58
12
14
52

Fig. 9

NANOIMPRINT LITHOGRAPHY

BACKGROUND OF THE INVENTION

The present invention relates to the lithography of the type used to produce integrated circuits and microdevices. More specifically, the present invention relates to a process that creates patterns with ultra fine features in a thin film carried on a surface of a substrate.

In fabrication of semiconductor integrated electrical circuits, integrated optical, magnetic, mechanical circuits and microdevices, and the like, one of the key processing methods is the lithography. Lithography creates a pattern in a thin film carried on a substrate so that, in subsequent process steps, the pattern will be replicated in the substrate or in another material which is added onto the substrate. Since the role of the thin film is to protect a part of the substrate in the subsequent replication steps, the thin film is called resist.

A typical lithography process for the integrated circuits fabrication involves exposing a resist with a beam of energetic particles which are electrons, or photons, or ions, by either passing a flood beam through a mask or scanning a focused beam. The particle beam changes the chemical structure of the exposed area of the film, so that when immersed in a developer, either the exposed area or the unexposed area of the resist will be removed to recreate the patterns or its obverse of the mask or the scanning. The lithography resolution is limited by the wavelength of the particles, the particle scattering in the resist and the substrate, and the properties of the resist.

There is an ongoing need in art of lithography to produce progressively smaller pattern size. There is a great need to develop low-cost technologies for mass producing sub-50 nm structures since such a technology could have an enormous impact in many areas of engineering and science. Not only will the future of semiconductor integrated circuits be affected, but the commercialization of many innovative electrical, optical, magnetic, mechanical microdevices that are far superior to current devices will rely on the possibility of such technology.

Numerous technologies have been developed to service this need, but they all suffer serious drawbacks and none of them can mass produce sub-50 nm lithography at a low cost. Electron beam lithography has demonstrated 10 nm lithography resolution. A. N. Broers, J. M. Harper, and W. W. Molzen, Appl. Phys. Lett. 33, 392 (1978) and P. B. Fischer and S. Y. Chou, Appl. Phys. Lett. 62, 2989 (1993). But using it for mass production of sub-50 nm structures seems economically impractical due to inherent low throughput in a serial processing tool. X-ray lithography, which can have a high throughput, has demonstrated 50 nm lithography resolution. K. Early, M. L. Schattenburg, and H. I. Smith, Microelectronic Engineering 11, 317 (1990). But the X-ray lithography tools are rather expensive and its ability for mass producing sub-50 nm structures is yet to be seen. Furthermore, lithographies based on scanning probes have produced sub-10 nm structures in a very thin layer of materials. However, the practicality of such lithographies as a manufacturing tool is hard to judge at this point.

Imprint technology using compressive molding of thermoplastic polymers is a low cost mass manufacturing technology and has been around for several decades. Features with sizes greater than 1 micrometers have been routinely imprinted in plastics. Compact disks which are based on imprinting of polycarbonate are one example. Other examples are imprinted polymethyl methacrylate (PMMA)

structures with a feature size on the order to 10 micrometers for making micromechanical parts. M. Harmening, W. Bacher, P. Bley, A. El-Kholi, H. Kalb, B. Kowanz, W. Menz, A. Michel, and J. Mohr, Proceedings IEEE Micro Electro Mechanical Systems, 202 (1992). Molded polyester micromechanical parts with feature dimensions of several tens of microns have also been used. H. Li and S. D. Senturia, Proceedings of 1992 13th IEEE/CHMT International Electronic Manufacturing Technology Symposium, 145 (1992). However, no one has recognized the use of imprint technology to provide 25 nm structures with high aspect ratios. Furthermore, the possibility of developing a lithographic method that combines imprint technology and other technologies to replace the conventional lithographies used in semiconductor integrated circuit manufacturing has never been raised.

SUMMARY OF THE INVENTION

The present invention relates to a method and apparatus for performing ultra-fine line lithography of the type used to produce integrated circuits and microdevices. A layer of thin film is deposited upon a surface of a substrate. A mold having at least one protruding feature and a recess is pressed into the thin film, therefore the thickness of the film under the protruding feature is thinner than the thickness of the film under the recess and a relief is formed in the thin film. The relief generally conforms to the shape of the feature on the mold. After mold is removed from the film, the thin film is processed such that the thinner portion of the film in the relief is removed exposing the underlying substrate. Thus, the patterns in the mold is replicated in the thin film, completing the lithography. The patterns in the thin film will be, in subsequent processes, reproduced in the substrate or in another material which is added onto the substrate.

The invention described here is based on a fundamentally different principle from conventional lithographies. The invention can eliminate many resolution limitations imposed in conventional lithographies, such as wavelength limitation, backscattering of particles in the resist and substrate, and interferences. It has been demonstrated the present invention is a high throughput mass production lithography method for generating sub-25 nm features. Furthermore, the present invention has the ability to mass produce 10 nm features at a low cost. These capabilities of the present invention is unattainable with the prior art.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A is a cross sectional view showing a mold and substrate in accordance with the present invention.

FIG. 1B is a cross sectional view of the mold and substrate of FIG. 1A showing the mold pressed into a thin film carried on the substrate.

FIG. 1C is a cross sectional view of the substrate of FIG. 1B following compression of the mold into the thin film.

FIG. 1D is a cross sectional view of the substrate of FIG. 1C showing removal of compressed portions of the thin film to expose the underlying substrate.

FIG. 2 is a scanning electron micrograph of a top view of 25 nm diameter holes with a 120 nm period formed by compressive molding into a PMMA film as shown in FIG. 1C.

FIG. 3 is a scanning electron micrograph of a top view of a 100 nm wide trench formed by compressive molding into a PMMA film as shown in FIG. 1C.

FIG. 4 is a scanning electron micrograph of a perspective view of the strips formed by compressive molding into a

PMMA film as shown in FIG. 1C. The strips are 70 nm wide and 200 nm tall, and have a high aspect ratio, a surface roughness less than 3 nm, and corners of nearly a perfect 90 degrees.

FIG. 5A is a cross sectional view of the substrate of FIG. 1D following deposition of a material.

FIG. 5B is a cross sectional view of the substrate of FIG. 5A following selective removal of the material by a lift off process.

FIG. 6 is a scanning electron micrograph of the substrate of FIG. 2 following deposition of material and a lift off process. The metal dots have a 25 nm diameter that is the same as that of the holes created in the PMMA shown in FIG. 2.

FIG. 7 is a scanning electron micrograph of the substrate of FIG. 3 following deposition of material and a lift off process. The metal linewidth is 100 nm that is the same as the width of the PMMA trenches shown in FIG. 3.

FIG. 8 is a cross sectional view of the substrate of FIG. 1D following subsequent processing.

FIG. 9 is a simplified block diagram of a apparatus in accordance with one embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This invention relates to a method and apparatus for a high-resolution, high-throughput, low-cost lithography. Unlike current microlithographies, the present invention abandons usage of energetic light or particle beams. Instead, the present invention is based on pressing a mold into a thin film on a substrate to create a relief and, later removing the compressed area of the film to expose the underlying substrate and to form a resist pattern on the substrate that replicates the obverse of the protruding pattern of the mold.

The present invention has demonstrated the generation of patterns, such as holes, pillars, or trenches in a thin film on a substrate, that have a minimum size of 25 nm, a depth over 100 nm, a side wall smoothness better than 3 nm, and corners with near perfect 90 degrees angles. It was found that presently the size of imprinted features is limited by the size of the mold being used; with a suitable mold, the present invention should create sub-10 nm structures with a high aspect ratio. Furthermore, using one embodiment of the present invention that including a material deposition and a lift-off process, 100 nm wide metal lines of a 200 nm period and 25 nm diameter metal dots of 125 nm period have been fabricated. The resist pattern created using the present invention also has been used as a mask to etch nanostructures into the substrate.

The present invention offers many unique advantages over the prior art. First, since it is based on a paradigm different from the prior art and it abandons the usage of an energetic particle beam such as photons, electrons, and ions, the present invention eliminates many factors that limit the resolution of conventional lithographies, such as wave diffraction limits due to a finite wavelength, the limits due to scattering of particles in the resist and the substrate, and interferences. Therefore the present invention offers a finer lithography resolution and much more uniform lithography over entire substrate than the prior art. My results show it can achieve sub-25 nm resolution. Second, the present invention can produce sub-25 nm features in parallel over a large area, leading to a high throughput. This seems unachievable with the prior art. And thirdly, since no sophisticated energetic particle beam generator is involved, the present invention can achieve a sub-25 nm lithography over a large area at a cost much lower than the prior art. These advantages make the present invention superior to the prior art and vital to future integrated circuit manufacturing and other areas of science and engineering where nanolithography is required.

FIGS. 1A–1D show steps in accordance with one embodiment. FIG. 1A shows mold **10** having body **12** and molding layer **14**. Molding layer **14** is shown as including a plurality of features **16** having a desired shape. A substrate **18** carries thin film layer **20**. Thin film layer **20** is deposited through any appropriate technique such as spin casting.

FIG. 1B shows a compressive molding step where mold **10** is pressed into thin film layer **20** in the direction shown by arrow **22** forming compressed regions **24**. In the embodiment shown in FIGS. 1A–1D, features **16** are not pressed all of the way into thin film **20** and do not contact substrate **18**. In some embodiments, top portions **24***a* of film **20** may contact depressed surfaces **16***a* of mold **10**. This causes top surfaces **24***a* to substantially conform to the shape of surfaces **16***a*, for example flat. When contact occurs, this also can stop the mold move further into the thin film **20**, due to a sudden increase of contact area and hence a decrease of the compressive pressure when the compressive force is constant.

FIG. 1C is a cross sectional view showing thin film layer **20** following removal of mold **10**. Layer **20** includes a plurality of recesses formed at compressed regions **24** which generally conform to the shape of features **16**. Layer **20** is subjected to a subsequent processing step as shown in FIG. 1D, in which the compressed portions **24** of film **20** are removed thereby exposing substrate **18**. This removal may be through any appropriate process such as reactive ion etching, wet chemical etching. This forms dams **26** having recesses **28** on the surface of substrate **18**. Recesses **28** form reliefs which conform generally to the shape of features **16** and mold **10**.

The mold **10** is patterned with features **16** comprising pillars, holes and trenches with a minimum lateral feature size of 25 nm, using electron beam lithography, reactive ion etching (RIE) and other appropriate methods. The typical depth of feature **16** is from 5 nm to 200 nm, depending upon the desired lateral dimension. In general, the mold should be selected to be hard relative to the softened thin film, and can be made of metals, dielectrics, or semiconductors or ceramics or their combination. In one experiment, the mold **10** consists of a layer **14** and features **16** of silicon dioxide on a silicon substrate **12**.

Thin film layer **20** comprises a thermoplastic polymer. During the compressive molding step shown in FIG. 1B, thin film **20** is heated at a temperature to allow sufficient softening of the film relative to the mold. For example, above the glass transition temperature the polymer has a low viscosity and can flow, thereby conforming to the features **16**.

In one experiment, the thin film **20** was a PMMA spun on a silicon wafer **18**. The thickness of the PMMA was chosen from 50 nm to 250 nm. PMMA was chosen for several reasons. First, PMMA does not adhere well to the SiO_2 mold due to its hydrophilic surface. Good mold release properties are essential for fabricating nanoscale features. Second, shrinkage of PMMA is less than 0.5% for large changes of temperature and pressure. See I. Rubin, *Injection Molding*, (Wiley, N.Y.) 1992. In a molding process, both the mold **10** and PMMA **20** were first heated to a temperature of 200° C. which is higher than the glass transition temperature of

PMMA, 105° C. See M. Harmening, W. Bacher, P. Bley, A. El-Kholi, H. Kalb, B. Kowanz, W. Menz, A. Michel, and J. Mohr, Proceedings IEEE Micro Electro Mechanical Systems, 202 (1992). Then the mold **10** and features **16** were compressed against the thin film **20** and held there until the temperature dropped below the PMMA's glass transition temperature. Various pressures have been tested. It was found that the one preferred pressure is about 1900 psi. At that pressure, the pattern of the features **16** can be fully transferred into the PMMA. After removing mold **10**, the PMMA in the compressed area was removed using an oxygen plasma, exposing the underlying silicon substrate and replicating the patterns of the mold over the entire thickness of the PMMA.

FIG. **2** shows a scanning electron micrograph of a top view of 25 nm diameter holes with a 120 nm period formed into a PMMA film in accordance with FIG. 1C. Mold features as large as tens of microns on the same mold as the nanoscale mold features have been imprinted.

FIG. **3** shows a scanning electron micrograph of a top view of 100 nm wide trenches with a 200 nm period formed in PMMA in accordance with FIG. 1C.

FIG. **4** is a scanning electron micrograph of a perspective view of trenches made in the PMMA using the present invention with embodiment that top portions **24***a* of film **20** contact depressed surfaces **16***a* of mold **10**. The strips are 70 nm wide, 200 nm tall, therefore a high aspect ratio. The surface of these PMMA features is extremely smooth and the roughness is less than 3 nm. The corners of the strips are nearly a perfect 90 degrees. Such smoothness, such sharp right angles, and such high aspect ratio at the 70 nm features size cannot be obtained with the prior art.

Furthermore, scanning electron microscopy of the PMMA patterns and the mold showed that the lateral feature size and the smoothness to the sidewalls of PMMA patterns fabricated using the present invention conform with the mold. From our observations, it is clear that the feature size achieved so far with the present invention is limited by our mold size. From the texture of the imprinted PMMA, it appears that 10 nm features can be fabricated with the present invention.

After the steps 1A–1D, the patterns in film **20** can be replicated in a material that is added on substrate **18** or can replicated directly into substrate **18**. FIGS. 5A and 5B show one example of the subsequent steps which follow the steps of FIGS. 1A–1D. Following formation of the recesses **28** shown in FIG. 1D, a layer of material **30** is deposited over substrate **18** as shown in FIG. 5A. Material **30** is deposited through any desired technique over dams **26** and into recesses **28** between dams **26**. Material **30** may comprise, for example, electrical conductors or semiconductors or dielectrics of the type used to fabricate integrated circuits, or it comprise ferromagnetic materials for magnetic devices. Next, a lift off process is performed in which a selective chemical etch is applied which removes dams **26** causing material **30** deposited on top of dams **26** to be removed. FIG. 5B shows the structure which results following the lift off process. A plurality of elements **32** formed of material **30** are left on the surface of substrate **18**. Elements **32** are of the type used to form miniaturized devices such as integrated circuits. Subsequent processing steps similar to those shown in steps 1A–1D may be repeated to form additional layers on substrate **18**.

FIG. **6** is a scanning electron micrograph of the substrate of FIG. **2** following deposition of 5 nm of titanium and 15 nm of gold and a lift off process. In the lift-off process, the wafers were soaked in acetone to dissolve the PMMA and therefore lift-off metals which were on the PMMA. The metal dots have a 25 nm diameter that is the same as that of the holes created in the PMMA using the present invention.

FIG. **7** is a scanning electron micrograph of the substrate of FIG. **3** following deposition of 5 nm of titanium and 15 nm of gold and a lift off process. The metal linewidth is 100 nm that is the same as the width of the PMMA trenches shown in FIG. **3**. FIGS. **6** and **7** have demonstrated that, during the oxygen RIE process in the present invention, the compressed PMMA area was completely removed and the lateral size of the PMMA features has not been changed significantly.

FIG. **8** is a cross sectional view of substrate **18** of FIG. 1D following an example alternative processing step that replicates the patterns in film **20** directly into substrate **18**. In FIG. **8**, substrate **18** has been exposed to an etching process such as reactive ion etching, chemical etching, etc., such that recesses **40** are formed in substrate **18**. These recesses **40** may be used for subsequent processing steps. For example, recesses **40** may be filled with material for use in fabricating a device. This is just one example of a subsequent processing step which can be used in conjunction with the present invention.

Molding processes typically use two plates to form malleable material therebetween. In the present invention, substrate **18** and body **12** (mold **10**) act as plates for the imprint process of the invention. Substrate **18** and body **12** should be sufficiently stiff to reduce bending while forming the imprint. Such bending leads to deformation in the pattern formed in the film **20**.

FIG. **9** is a simplified block diagram of apparatus **50** for performing nanoimprint lithography in accordance with the invention. Apparatus **50** includes stationary block **52** carrying substrate **18** and moveable molding block **54** carrying mold **10**. Blocks **52** and **54** carry the substrate **18** and mold **10** depicted in FIGS. 1A–1D. A controller **56** couples to x-y positioner **58** and z positioner **60**. An alignment mark **64** is on mold **10** and complimentary mark **68** is on substrate **18**. Sensor **62** carried in block **54** couples to alignment marks **64** and **68** and provide an alignment signal to controller **56**. Controller **56** is also provided with input output circuitry **66**.

In operation, controller **56** controls the imprinting of mold **10** into film **20** on substrate **18** by actuating z positioner **60** which moves block **54** in the z direction relative to block **52**. During the imprinting process, precise alignment of mold **10** and film **20** is crucial. This is achieved using optical or electrical alignment techniques. For example, sensor **62** and alignment marks **64** and **68** may be an optical detector and optical alignment marks which generate a moiré alignment pattern such that moiré alignment techniques may be employed to position mold **10** relative to film **20**. Such techniques are described by Nomura et al. A MOIRÉ ALIGNMENT TECHNIQUE FOR MIX AND MATCH LITHOGRAPHIC SYSTEM, J. Vac. Sci. Technol. B6(1), Jan/Feb 1988, pg. 394 and by Hara et al., AN ALIGNMENT TECHNIQUE USING DEFRACTED MOIRE SIGNALS J. Vac. Sci, Technol. B7(6), Nov/Dec 1989, pg. 1977. Controller **56** processes this alignment information and adjusts the position of block **54** in the x-y plane relative to film **20** using x-y positioner **58**. In another embodiment, alignment marks **64** and **68** comprise plates of a capacitor such that sensor **62** detects capacitance between marks **64** and **68**. Using this technique, alignment is achieved by moving block **54** in the x-y plane to maximize the capacitance between alignment marks **64** and **68**. During imprinting, controller **56** may also monitor and control the temperature of film **20**.

It should be understood that the invention is not limited to the specific technique described herein, and may be implemented in any appropriate lithographic process. Generally, the mold should be hard relative to the film during the molding process. This may be achieved for example, by sufficiently heating the film. Additionally, it should be understood that the invention is not limited to the particular film described herein. For example, other types of films may be used. In one alternative embodiment, a thin film may be developed which has a chemical composition which changes under pressure. Thus, following the imprint process, a chemical etch could be applied to the film which selectively etches those portions whose composition had changed due to applied pressure. In another embodiment, after molding of the thin film to create a thickness contrast in the thin film, a material is deposited on the thin film and the thickness contrast then is transferred into the substrate.

Although the present invention has been described with reference to preferred embodiments, workers skilled in the art will recognize that changes may be made in form and detail without departing from the spirit and scope of the invention.

What is claimed is:

1. A lithographic method for forming a pattern in a film carried on a substrate, comprising the steps of:

obtaining a substrate;

depositing a film on the substrate;

obtaining a mold of a stiff material which is hard relative to the film, the mold having a first protruding feature and a recess formed thereby and a second protruding feature spaced apart prom the first protruding feature, the first and second features and the recess having a shape forming a mold pattern and providing at least one mold pattern lateral dimension which is less than 200 nm;

urging the mold at a molding pressure into the film whereby the thickness of the film under the protruding feature is reduced and a thin region is formed in the film, wherein the molding pressure is sufficiently high to transfer the mold pattern to the film and the molding pressure causes a local deformation in the mold which is less than the mold pattern lateral dimension;

removing the mold from the film;

processing the relief whereby the thin region is removed exposing portions of the surface of the substrate which underlie the thin region; and

whereby the exposed portions of the surface of the substrate substantially replicate the mold pattern and have at least one lateral dimension which is less than 200 nm.

2. The method of claim 1 wherein the thin film comprises a thermoplastic polymer.

3. The method of claim 1 including heating the thin film to a temperature to allow sufficient softening of the film relative to the mold prior to the step of urging.

4. The method of claim 1 wherein the features on the mold are formed from material selected from the group consisting of: semiconductors, dielectrics, metals, and their combination.

5. The method of claim 1 wherein the step of urging comprises pressing the mold into the thin film without allowing the features to contact the underlying substrate.

6. The method of claim 1 wherein the step of processing comprises reactive ion etching.

7. The method of claim 1 including repeating the steps of obtaining a mold, urging, removing, and processing to form a multilayered device.

8. The method of claim 1 including the step of aligning the features on the mold with a pattern on the substrate.

9. The method of claim 1 including the step of depositing a material on the exposed portion of the substrate.

10. The method of claim 9 wherein the material is selected from the group consisting of semiconductors, dielectrics, metals, and their combination.

11. The method of claim 9 including selectively removing the film following depositing the material.

12. The method of claim 11 wherein the step of selectively removing the film comprises a lift off process.

13. The method of claim 1 including removing the exposed portion of the substrate to form a recess in the substrate.

14. A lithographic method for forming a pattern in a film carried on a substrate, comprising the steps;

obtaining a substrate;

depositing a thin film on the substrate;

obtaining a mold of a stiff material which is hard relative to the film, the mold having a first feature and a second feature, the first feature spaced apart from the second feature, the first and second features forming a mold pattern having at least one mold pattern lateral dimension which is less than 200 nm;

molding the film with the features of the mold to form thin regions in the film shaped by the features by pressing the mold into the film at a molding pressure, wherein the pressure is sufficiently high to transfer the features to the film and the molding pressure causes a local deformation in the mold which is less than the mold pattern lateral dimension; and

removing the thin region of the film exposing portions of the substrate underlying the thin regions thereby patterning the substrate with the feature to form a pattern which has at least one lateral dimension which is less than 200 nm.

15. The method of claim 14 including the step of depositing a material on the exposed portion of the substrate.

16. The method of claim 14 including removing the exposed portion of the substrate to form a recess in the substrate.

17. The method of claim 14 including repeating the steps of obtaining a mold, molding and removing to form a multilayered device.

18. The method of claim 14 including the step of aligning the features on the mold with a pattern on the substrate.

19. A lithographic method for forming a pattern in a film carried on a substrate, comprising the steps of:

obtaining a substrate;

depositing a film on the substrate;

obtaining a mold of a stiff material which is hard relative to the film, the mold having a first protruding feature and a recess formed thereby, and a second protruding feature spaced apart from the first protruding feature, the features and the recess having a shape forming a mold pattern with at least one mold pattern lateral dimension which is less than 200 nm;

urging the mold at a molding pressure into the film creating a thickness contrast pattern in the film, wherein the molding pressure is sufficiently high to transfer the features to the film and the molding pressure causes a local deformation in the mold which is less than the mold pattern lateral dimension;

removing the mold from the film; and

transferring the thickness contrast pattern in the film onto the substrate wherein the thickness contrast has at least one lateral dimension which is less than 200 nm.

* * * * *